

PCI Routing

	IDSEL	IRQ	REQ/GNT
MiniPCI	21	F	0
LAN	23	H	2
7411	22	E (CardBus)	1
7411	22	G (1394)	1
7411	22	E (FlashMedia)	1

Ref. function schematic BOM

U81 cpu socket 62.10055.091 (DON'T CHANGE) (3mm high)
U80 north bridge 71.RS48M.00U 71.RS48M.B0U (ver A22)
U43 south bridge 71.SB400.B0U 71.SB400.D0U (ver A32)
U32 clock gen. 71.00137.A0W 71.00137.B0W

U70 VGA M24 71.0M26P.00U 71.00M24.C0U
U64 VRAM FOR M24 72.55732.B0U 72.52832.E05
U65 VRAM FOR M24 72.55732.B0U 72.52832.E05
U69 VRAM FOR M24 72.55732.B0U 72.52832.E05
U71 VRAM FOR M24 72.55732.B0U 72.52832.E05

U70 VGA M26 71.0M26P.00U (DON'T CHANGE)
U64 VRAM FOR M26 72.55732.B0U (DON'T CHANGE)
U65 VRAM FOR M26 72.55732.B0U (DON'T CHANGE)
U69 VRAM FOR M26 72.55732.B0U (DON'T CHANGE)
U71 VRAM FOR M26 72.55732.B0U (DON'T CHANGE)

U66 BIOS SOCKET 72.39040.G03 62.10002.032 (NO NEED WHEN PD)
U66 BIOS IC 72.39040.G03 72.39040.H03 (DIP STAGE IN LAB, SMT IN PD)

LOUT1 AUDIO 22.10257.001 22.10147.031 (NO SPDIF)

U75 GIGA LAN 71.08110.00G 71.08110.A0G
U75 10/100 LAN 71.08110.00G 71.08100.C0G

HDD1 20.80175.044 20.80592.044
SATA1 20.F0614.022 20.F0665.022
EZ4 20.80579.120 20.80591.120 (AFTER SB)

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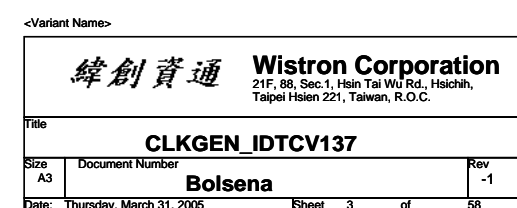
<Variant Name>

緯創資通

Wistron Corporation

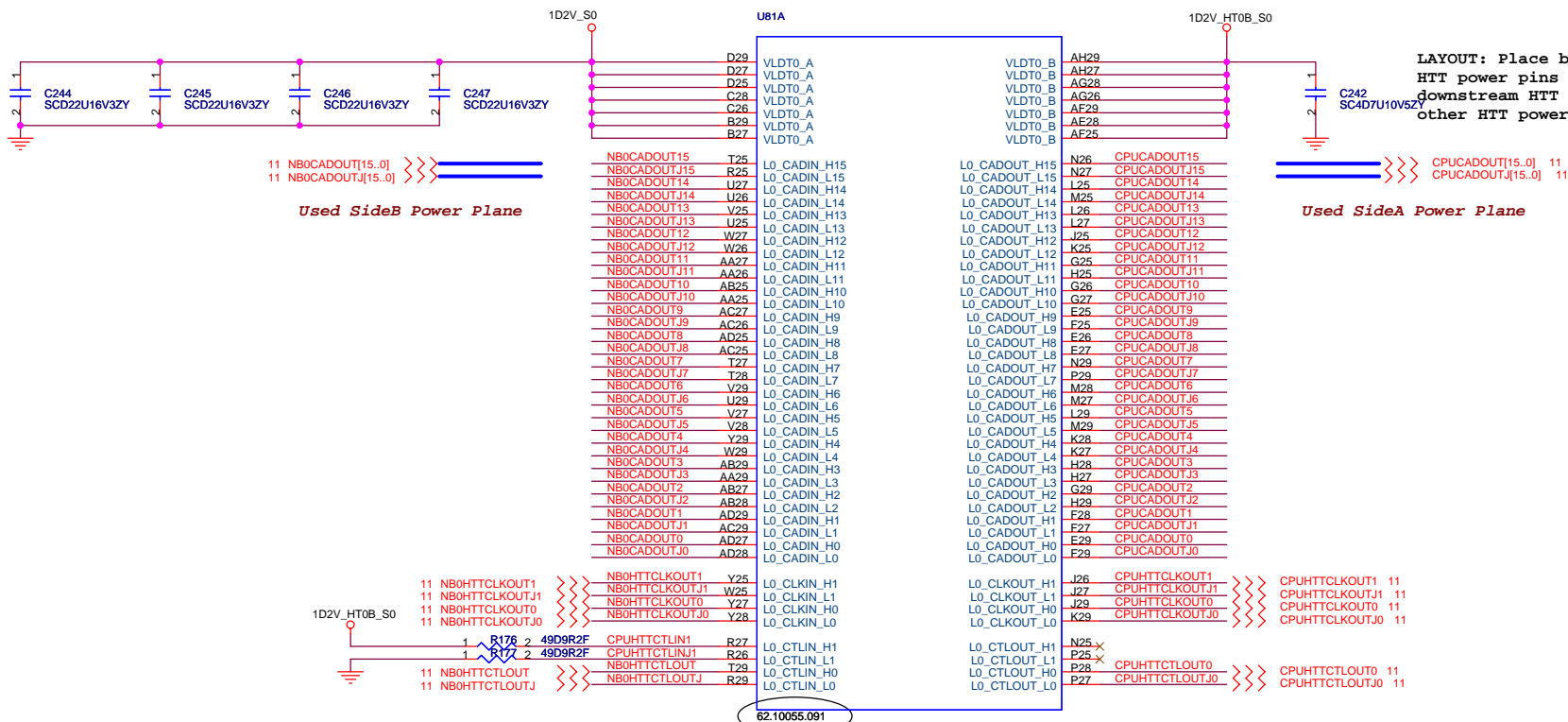
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Title			CHANGE HISTORY		
Size	Document Number				Rev
A3	Bolsena				1
Date: Thursday, March 31, 2005			Sheet	2	of 58



HTT for CPU sideA
Transmit power
and NB sideA Receive
power

HTT for CPU sideB
Receive power
and NB sideA
Transmit power



LAYOUT: Place bypass cap on topside of board near
HTT power pins that are not connected directly to
downstream HTT device, but connected internally to
other HTT power pins.

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU(1/4)_HyperTransport I/F

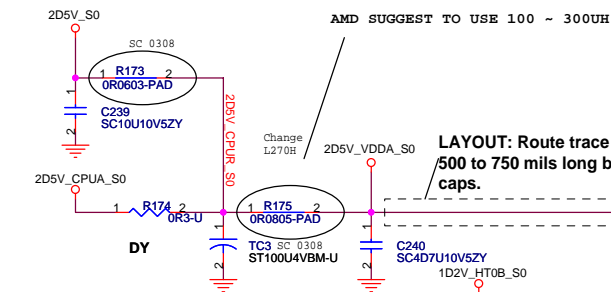
Size A3 Document Number

Bolsena

Date: Thursday, March 31, 2005 Sheet 4 of 58

Rev -1

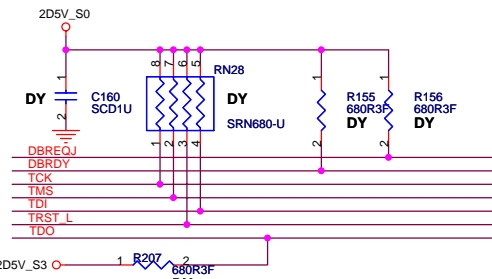
2D5V_VDDA_S0



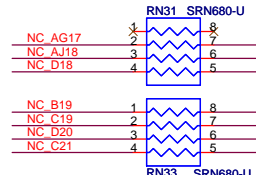
AMD SUGGEST TO USE 2D5V_CPUA_S0

KEMET, NT: 5.7, B2 size
ST100U4VBM-1 (80.10716.321)
I_{ripple} = 1.1A, ESR = 70mohm
SANYO, NT: 6.1
I_{ripple} = 1.1A, ESR = 70mohm
3.5/2.8/2.0
77.21071.031

AMD suggest voltage
from 2D5V_S0 to 2D5V_S3
differentially impedance 100



CHANGE FROM 1KR3 TO 680R2 FOR AMD
CHECK LIST

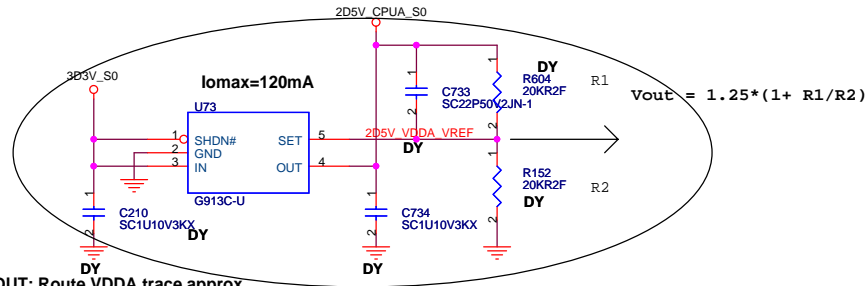


Validation Test Points

LAYOUT: Place close to the CPU.

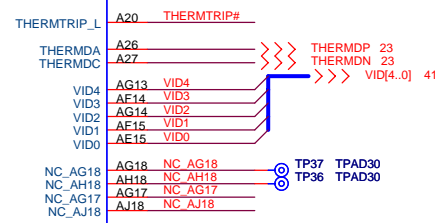
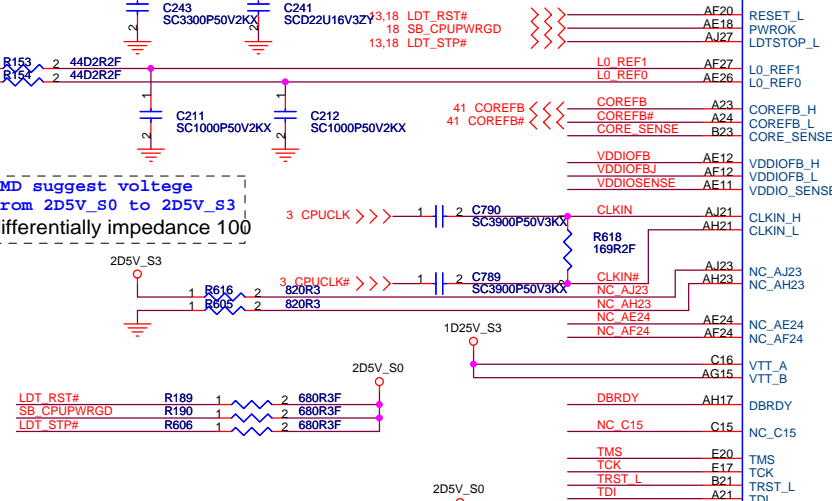
NC C15	TP56	TPAD30
NC AE23	TP42	TPAD30
NC AF23	TP39	TPAD30
NC AF22	TP41	TPAD30
NC AF21	TP40	TPAD30

LDT_RST#	TP38	TPAD30
CLKIN#	TP34	TPAD30
CORE_SENSE	TP35	TPAD30
VDDIOFB	TP43	TPAD30
VDDIOFBJ	TP46	TPAD30
VDDIOSENSE	TP45	TPAD30
NC AE24	TP48	TPAD30
NC AF24	TP27	TPAD30
	TP26	TPAD30

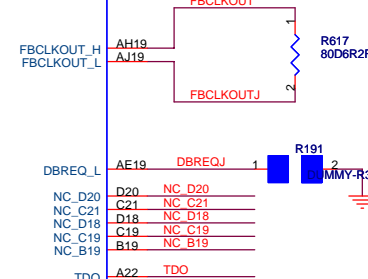


LAYOUT: Route trace 50 mils wide and
500 to 750 mils long between these
caps.

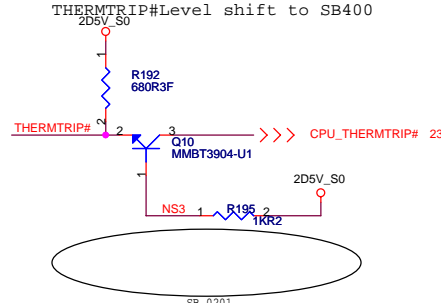
LAYOUT: Route VDDA trace approx.
50 mils wide (use 2x25 mil traces to
exit ball field) and 500 mils long.



LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80



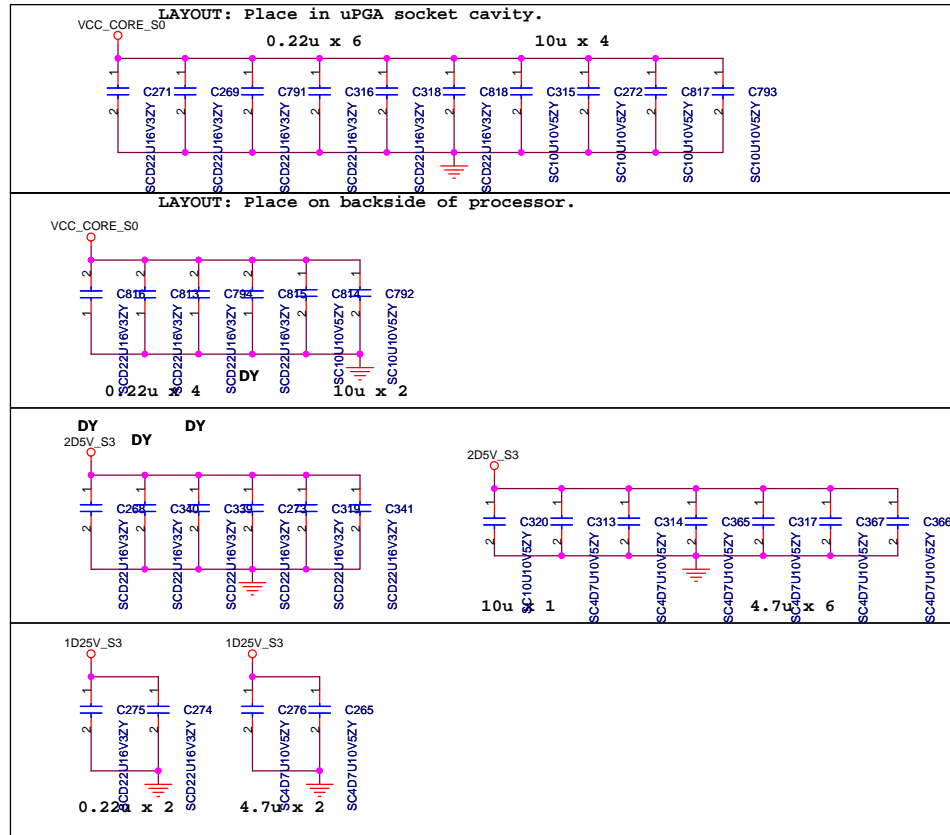
Connect to VDDIO for AMD suggest.



<Variant Name>

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Title		
CPU(3/4)_Control & Debug		
Size	Document Number	Rev
A3	Bolsena	-1
Date:	Thursday, March 31, 2005	Sheet 6 of 58



M_AA0 112
M_AA1 111
M_AA2 110
M_AA3 109
M_AA4 108
M_AA5 107
M_AA6 106
M_AA7 105
M_AA8 102
M_AA9 101
M_AA10 115
M_AA11 100
M_AA12 99

M_ABS#0 117
M_ABS#1 116

M_DATA R 0 5
M_DATA R 1 7
M_DATA R 2 13
M_DATA R 3 17
M_DATA R 4 6
M_DATA R 5 8
M_DATA R 6 14
M_DATA R 7 18
M_DATA R 8 19
M_DATA R 9 23
M_DATA R 10 29
M_DATA R 11 31
M_DATA R 12 20
M_DATA R 13 24
M_DATA R 14 30
M_DATA R 15 32
M_DATA R 16 41
M_DATA R 17 43
M_DATA R 18 49
M_DATA R 19 53
M_DATA R 20 42
M_DATA R 21 44
M_DATA R 22 50
M_DATA R 23 54
M_DATA R 24 55
M_DATA R 25 59
M_DATA R 26 65
M_DATA R 27 67
M_DATA R 28 56
M_DATA R 29 66
M_DATA R 30 66
M_DATA R 31 68
M_DATA R 32 127
M_DATA R 33 129
M_DATA R 34 135
M_DATA R 35 139
M_DATA R 36 128
M_DATA R 37 130
M_DATA R 38 136
M_DATA R 39 140
M_DATA R 40 141
M_DATA R 41 145
M_DATA R 42 151
M_DATA R 43 153
M_DATA R 44 142
M_DATA R 45 146
M_DATA R 46 152
M_DATA R 47 154
M_DATA R 48 165
M_DATA R 49 163
M_DATA R 50 171
M_DATA R 51 175
M_DATA R 52 164
M_DATA R 53 166
M_DATA R 54 172
M_DATA R 55 176
M_DATA R 56 177
M_DATA R 57 181
M_DATA R 58 187
M_DATA R 59 189
M_DATA R 60 178
M_DATA R 61 182
M_DATA R 62 188
M_DATA R 63 190

CB0 71
CB1 73
CB2 79
CB3 83
CB4 72
CB5 74
CB6 80
CB7 84
NC#85
NC#86/(RESET#)
NC#97/A13
NC#98/BA2
NC#123
NC#124
NC#200

/RAS 118
/CAS 120
/WE 119
VREF_DDR_MEM 1
VREF 2
VREF 197
VDDSPD 199
VDDID 201
GND 202

5.9 M_ARAS#
5.9 M_ACAS#
5.9 M_AWE#

Layout trace 20 mil
C458 SCD1U
TP62

/CS0 121
/CS1 122
M_CKE#0 96
M_CKE#1 95
M_DQS R0 11
M_DQS R1 25
M_DQS R2 47
M_DQS R3 61
M_DQS R4 133
M_DQS R5 147
M_DQS R6 169
M_DQS R7 183
M_BBS#0 117
M_BBS#1 116

M_ADM#0 12
M_ADM#1 26
M_ADM#2 48
M_ADM#3 62
M_ADM#4 134
M_ADM#5 148
M_ADM#6 170
M_ADM#7 184

M_CLK#5 5
M_CLK#6 5
M_CLK#7 5
DDR CLK0
DDR CLK#0

SMBC_SB 195
SMBD_SB 193

SA0 194
SA1 196
SA2 198
VDD 9
VDD 10
VDD 21
VDD 22
VDD 33
VDD 34
VDD 36
VDD 45
VDD 46
VDD 57
VDD 58
VDD 69
VDD 70
VDD 81
VDD 82
VDD 92
VDD 93
VDD 94
VDD 113
VDD 114
VDD 131
VDD 132
VDD 143
VDD 144
VDD 155
VDD 156
VDD 167
VDD 168
VDD 179
VDD 180
VDD 191
VDD 192

NOT SUPPORT ECC CHECK
AMD suggested pull-low

2D5V_S3

1ST 62.10017.701 - 2ND 62.10017.201

Part Number = 62.10017.201
DDR-SODIMM-R-U2

ME : 62.10017.201
2nd : 62.10017.701

M_BA0 112
M_BA1 111
M_BA2 110
M_BA3 109
M_BA4 108
M_BA5 107
M_BA6 106
M_BA7 105
M_BA8 102
M_BA9 101
M_BA10 115
M_BA11 100
M_BA12 99

M_BBS#0 117
M_BBS#1 116

M_DATA R 0 5
M_DATA R 1 7
M_DATA R 2 13
M_DATA R 3 17
M_DATA R 4 6
M_DATA R 5 8
M_DATA R 6 14
M_DATA R 7 18
M_DATA R 8 19
M_DATA R 9 23
M_DATA R 10 29
M_DATA R 11 31
M_DATA R 12 20
M_DATA R 13 24
M_DATA R 14 30
M_DATA R 15 32
M_DATA R 16 41
M_DATA R 17 43
M_DATA R 18 49
M_DATA R 19 53
M_DATA R 20 42
M_DATA R 21 44
M_DATA R 22 50
M_DATA R 23 54
M_DATA R 24 55
M_DATA R 25 59
M_DATA R 26 65
M_DATA R 27 67
M_DATA R 28 56
M_DATA R 29 66
M_DATA R 30 66
M_DATA R 31 68
M_DATA R 32 127
M_DATA R 33 129
M_DATA R 34 135
M_DATA R 35 139
M_DATA R 36 128
M_DATA R 37 130
M_DATA R 38 136
M_DATA R 39 140
M_DATA R 40 141
M_DATA R 41 145
M_DATA R 42 151
M_DATA R 43 153
M_DATA R 44 142
M_DATA R 45 146
M_DATA R 46 152
M_DATA R 47 154
M_DATA R 48 165
M_DATA R 49 163
M_DATA R 50 171
M_DATA R 51 175
M_DATA R 52 164
M_DATA R 53 166
M_DATA R 54 172
M_DATA R 55 176
M_DATA R 56 177
M_DATA R 57 181
M_DATA R 58 187
M_DATA R 59 189
M_DATA R 60 178
M_DATA R 61 182
M_DATA R 62 188
M_DATA R 63 190

SA0 194
SA1 196
SA2 198
VDD 9
VDD 10
VDD 21
VDD 22
VDD 33
VDD 34
VDD 36
VDD 45
VDD 46
VDD 57
VDD 58
VDD 69
VDD 70
VDD 81
VDD 82
VDD 92
VDD 93
VDD 94
VDD 113
VDD 114
VDD 131
VDD 132
VDD 143
VDD 144
VDD 155
VDD 156
VDD 167
VDD 168
VDD 179
VDD 180
VDD 191
VDD 192

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AMD suggested pull-low

2D5V_S3

1ST 62.10017.701 - 2ND 62.10017.201

Part Number = 62.10017.201
DDR-SODIMM-R-U2

ME : 62.10017.201
2nd : 62.10017.701

/CS0 121
/CS1 122
M_CKE#0 96
M_CKE#1 95
M_DQS R0 11
M_DQS R1 25
M_DQS R2 47
M_DQS R3 61
M_DQS R4 133
M_DQS R5 147
M_DQS R6 169
M_DQS R7 183
M_BBS#0 117
M_BBS#1 116

M_ADM#0 12
M_ADM#1 26
M_ADM#2 48
M_ADM#3 62
M_ADM#4 134
M_ADM#5 148
M_ADM#6 170
M_ADM#7 184

M_CLK#4 5
M_CLK#5 5
M_CLK#6 5
DDR CLK1
DDR CLK#1

SMBC_SB 3.21
SMBD_SB 3.21

DM SA0 1
R312 4K7R2
3D3V_S0

2D5V_S3

1ST 62.10017.701 - 2ND 62.10017.201

Part Number = 62.10017.201
DDR-SODIMM-R-U2

ME : 62.10017.201
2nd : 62.10017.701

M_BA0 112
M_BA1 111
M_BA2 110
M_BA3 109
M_BA4 108
M_BA5 107
M_BA6 106
M_BA7 105
M_BA8 102
M_BA9 101
M_BA10 115
M_BA11 100
M_BA12 99

M_BBS#0 117
M_BBS#1 116

M_DATA R 0 5
M_DATA R 1 7
M_DATA R 2 13
M_DATA R 3 17
M_DATA R 4 6
M_DATA R 5 8
M_DATA R 6 14
M_DATA R 7 18
M_DATA R 8 19
M_DATA R 9 23
M_DATA R 10 29
M_DATA R 11 31
M_DATA R 12 20
M_DATA R 13 24
M_DATA R 14 30
M_DATA R 15 32
M_DATA R 16 41
M_DATA R 17 43
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M_DATA R 20 42
M_DATA R 21 44
M_DATA R 22 50
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M_DATA R 24 55
M_DATA R 25 59
M_DATA R 26 65
M_DATA R 27 67
M_DATA R 28 56
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M_DATA R 31 68
M_DATA R 32 127
M_DATA R 33 129
M_DATA R 34 135
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M_DATA R 46 152
M_DATA R 47 154
M_DATA R 48 165
M_DATA R 49 163
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M_DATA R 51 175
M_DATA R 52 164
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M_DATA R 54 172
M_DATA R 55 176
M_DATA R 56 177
M_DATA R 57 181
M_DATA R 58 187
M_DATA R 59 189
M_DATA R 60 178
M_DATA R 61 182
M_DATA R 62 188
M_DATA R 63 190

SA0 194
SA1 196
SA2 198
VDD 9
VDD 10
VDD 21
VDD 22
VDD 33
VDD 34
VDD 36
VDD 45
VDD 46
VDD 57
VDD 58
VDD 69
VDD 70
VDD 81
VDD 82
VDD 92
VDD 93
VDD 94
VDD 113
VDD 114
VDD 131
VDD 132
VDD 143
VDD 144
VDD 155
VDD 156
VDD 167
VDD 168
VDD 179
VDD 180
VDD 191
VDD 192

NOT SUPPORT ECC CHECK
AMD suggested pull-low

2D5V_S3

1ST 62.10017.701 - 2ND 62.10017.201

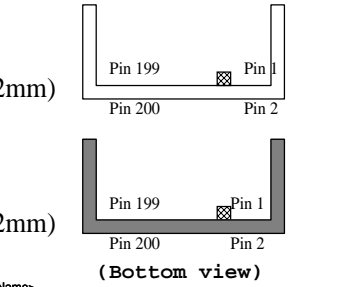
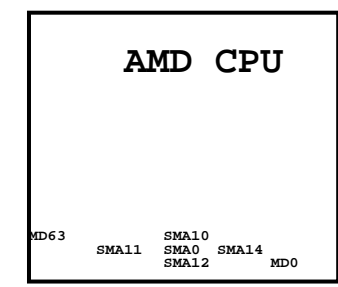
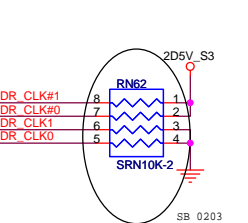
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DDR-SODIMM-R-U2

ME : 62.10017.201
2nd : 62.10017.701

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M_ADM#1 26
M_ADM#2 48
M_ADM#3 62
M_ADM#4 134
M_ADM#5 148
M_ADM#6 170
M_ADM#7 184

M_CLK#4 5
M_CLK#5 5
M_CLK#6 5
DDR CLK1
DDR CLK#1

SMBC_SB 3.21
SMBD_SB 3.21



AMD CPU

MD63 SMA11 SMA10 SMA14 MD0

Pin 199 Pin 1

Pin 200 Pin 2

Pin 199 Pin 1

Pin 200 Pin 2

(Bottom view)

<Variant Name>

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Title

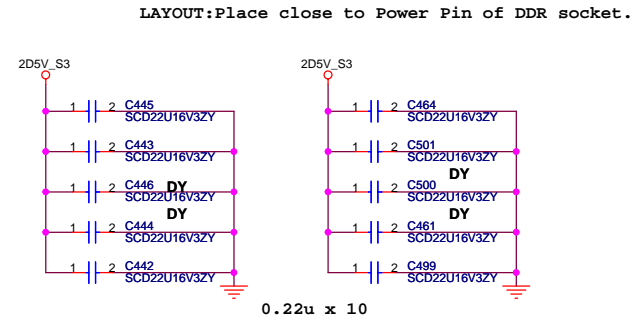
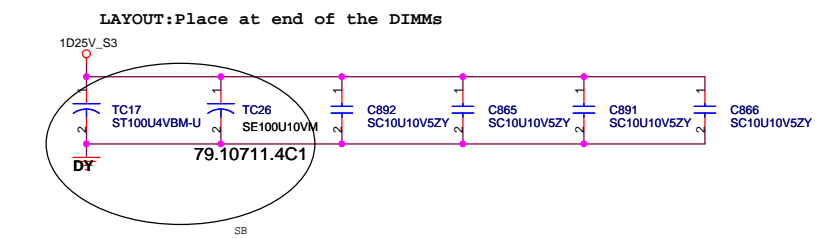
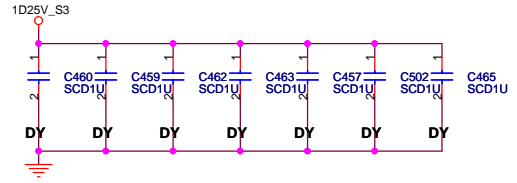
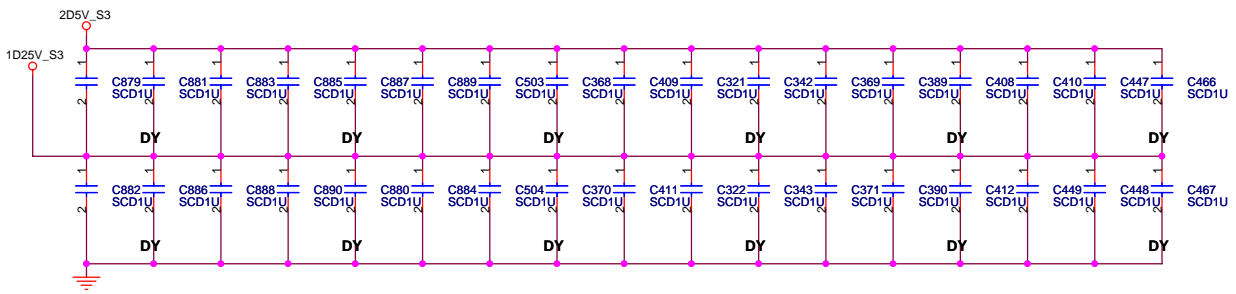
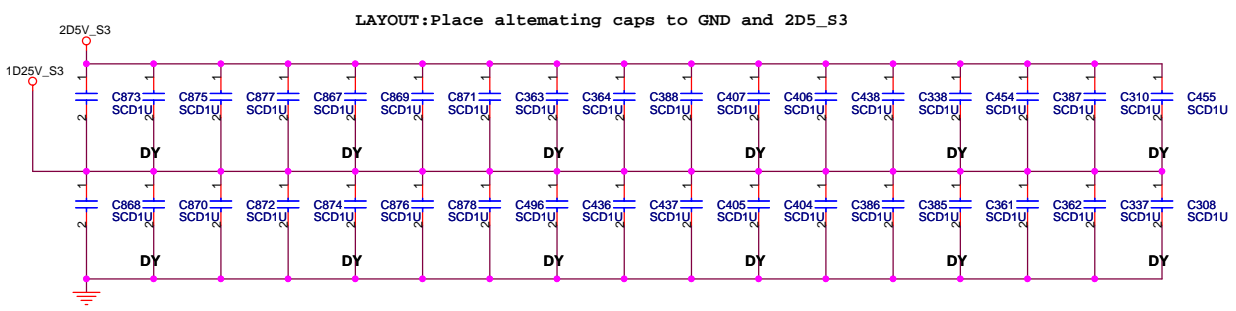
Size A3 Document Number

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Date: Thursday, March 31, 2005 Sheet 8 of 58

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Title			
DDR DAMPING & TERMINATION			
Size A3	Document Number Bolsena		Rev -1
Date: Thursday, March 31, 2005	Sheet 9	of 58	



CLAW HAMMER TO NB

NB TO CLAW HAMMER

4 CPUCADOUT[15..0] >>>
4 CPUCADOUTJ[15..0] >>>

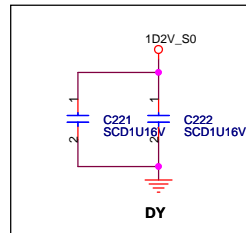
U80A
PART 10F6
CPUCADOUT15 T26 HT_RXCAD15P
CPUCADOUT15 R26 HT_RXCAD15N
CPUCADOUT14 U25 HT_RXCAD14P
CPUCADOUT14 U24 HT_RXCAD14N
CPUCADOUT13 V26 HT_RXCAD13P
CPUCADOUT13 U26 HT_RXCAD13N
CPUCADOUT12 W25 HT_RXCAD12P
CPUCADOUT12 W24 HT_RXCAD12N
CPUCADOUT11 AA25 HT_RXCAD11P
CPUCADOUT11 AA24 HT_RXCAD11N
CPUCADOUT10 AB26 HT_RXCAD10P
CPUCADOUT10 AA26 HT_RXCAD10N
CPUCADOUT9 AC25 HT_RXCAD9P
CPUCADOUT9 AC24 HT_RXCAD9N
CPUCADOUT8 AD26 HT_RXCAD8P
CPUCADOUT8 AC26 HT_RXCAD8N
CPUCADOUT7 R29 HT_RXCAD7P
CPUCADOUT7 R28 HT_RXCAD7N
CPUCADOUT6 T30 HT_RXCAD6P
CPUCADOUT6 R30 HT_RXCAD6N
CPUCADOUT5 T28 HT_RXCAD5P
CPUCADOUT5 T29 HT_RXCAD5N
CPUCADOUT4 V29 HT_RXCAD4P
CPUCADOUT4 U29 HT_RXCAD4N
CPUCADOUT3 Y30 HT_RXCAD3P
CPUCADOUT3 W30 HT_RXCAD3N
CPUCADOUT2 Y29 HT_RXCAD2P
CPUCADOUT2 Y28 HT_RXCAD2N
CPUCADOUT1 AB29 HT_RXCAD1P
CPUCADOUT1 AA29 HT_RXCAD1N
CPUCADOUT0 AC29 HT_RXCAD0P
CPUCADOUT0 AC28 HT_RXCAD0N

PART 10F6

HYPER TRANSPORT CPU I/F

HT_TXCAD15P R24 NB0CADOUT15
HT_TXCAD15N R25 NB0CADOUT15N
HT_TXCAD14P N26 NB0CADOUT14
HT_TXCAD14N P26 NB0CADOUT14N
HT_TXCAD13P N25 NB0CADOUT13
HT_TXCAD13N L26 NB0CADOUT12
HT_TXCAD12P M26 NB0CADOUT12
HT_TXCAD12N J26 NB0CADOUT11
HT_TXCAD11P K26 NB0CADOUT11
HT_TXCAD11N J24 NB0CADOUT10
HT_TXCAD10P J25 NB0CADOUT10
HT_TXCAD10N G26 NB0CADOUT9
HT_TXCAD9P H26 NB0CADOUT9
HT_TXCAD9N G24 NB0CADOUT8
HT_TXCAD8P G25 NB0CADOUT8
HT_TXCAD8N
HT_TXCAD7P L30 NB0CADOUT7
HT_TXCAD7N M30 NB0CADOUT7
HT_TXCAD6P L28 NB0CADOUT6
HT_TXCAD6N L29 NB0CADOUT6
HT_TXCAD5P J29 NB0CADOUT5
HT_TXCAD5N K29 NB0CADOUT5
HT_TXCAD4P H30 NB0CADOUT4
HT_TXCAD4N H29 NB0CADOUT4
HT_TXCAD3P E29 NB0CADOUT3
HT_TXCAD3N E28 NB0CADOUT3
HT_TXCAD2P D30 NB0CADOUT2
HT_TXCAD2N E30 NB0CADOUT2
HT_TXCAD1P D28 NB0CADOUT1
HT_TXCAD1N D29 NB0CADOUT1
HT_TXCAD0P B29 NB0CADOUT0
HT_TXCAD0N C29 NB0CADOUT0

NB0CADOUT[15..0] 4
NB0CADOUTJ[15..0] 4



AROUND NB

4 CPUHTTCLKOUT1 >>>
4 CPUHTTCLKOUTJ1 >>>

CPUHTTCLKOUT1 Y26 HT_RXCLK1P
CPUHTTCLKOUTJ1 W26 HT_RXCLK1N

HT_RXCLK1P
HT_RXCLK1N

HT_TXCLK1P L24 NB0HTTCLKOUT1
HT_TXCLK1N L25 NB0HTTCLKOUTJ1

NB0HTTCLKOUT1 4
NB0HTTCLKOUTJ1 4

4 CPUHTTCLKOUT0 >>>
4 CPUHTTCLKOUTJ0 >>>

CPUHTTCLKOUT0 W29 HT_RXCLK0P
CPUHTTCLKOUTJ0 W28 HT_RXCLK0N

HT_RXCLK0P
HT_RXCLK0N

HT_TXCLK0P F29 NB0HTTCLKOUT0
HT_TXCLK0N G29 NB0HTTCLKOUTJ0

NB0HTTCLKOUT0 4
NB0HTTCLKOUTJ0 4

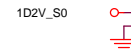
4 CPUHTTCTLOUT0 >>>
4 CPUHTTCTLOUTJ0 >>>

CPUHTTCTLOUT0 P29 HT_RXCTLP
CPUHTTCTLOUTJ0 N29 HT_RXCTLN

HT_RXCTLP
HT_RXCTLN

HT_TXCTLP M29 NB0HTTCTLOUT
HT_TXCTLN M28 NB0HTTCTLOUTJ

NB0HTTCTLOUT 4
NB0HTTCTLOUTJ 4



HT_RXCALN D27
HT_RXCALP E27

HT_RXCALN
HT_RXCALP

HT_TXCALP B28 HT_TXCALP
HT_TXCALN A28 HT_TXCALN



CHANGE TO 71.RS48M.B0U (VER A22)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

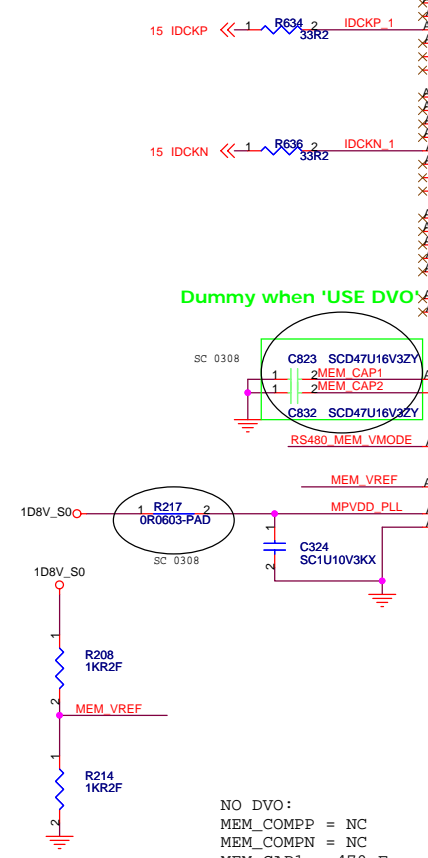
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Size	Document Number	Rev	
A3	Bolsena	-1	
Date:	Thursday, March 31, 2005	Sheet	11 of 58

49 PEG_TXP[15..0] <<< <<<
49 PEG_TXN[15..0] <<< <<<
49 PEG_RXP[15..0] >>> >>>
49 PEG_RXN[15..0] >>> >>>

PART 3 OF 6		
MEM_A0	MEM_DQ0	AE28
MEM_A1	MEM_DQ1	AE27
MEM_A2	MEM_DQ2	AG28
MEM_A3	MEM_DQ3	AE26
MEM_A4	MEM_DQ4	AE25
MEM_A5	MEM_DQ5	AE24
MEM_A6	MEM_DQ6	AE23
MEM_A7	MEM_DQ7	AE22
MEM_A8	MEM_DQ8	AE21
MEM_A9	MEM_DQ9	AE20
MEM_A10	MEM_DQ10	AG30
MEM_A11	MEM_DQ11	AG29
MEM_A12	MEM_DQ12	AE28
MEM_A13	MEM_DQ13	AE27
MEM_A14	MEM_DQ14	AE26
MEM_DM0	MEM_DQ15	AE25
MEM_DM1	MEM_DQ16	AE24
MEM_DM2	MEM_DQ17	AE23
MEM_DM3	MEM_DQ18	AE22
MEM_DM4	MEM_DQ19	AE21
MEM_DM5	MEM_DQ20	AE20
MEM_DM6	MEM_DQ21	AG19
MEM_DM7	MEM_DQ22	AG20
MEM_DQS0P	MEM_DQ23	AE19
MEM_DQS1P	MEM_DQ24	AE18
MEM_DQS2P	MEM_DQ25	AE17
MEM_DQS3P	MEM_DQ26	AE16
MEM_DQS4P	MEM_DQ27	AE15
MEM_DQS5P	MEM_DQ28	AE14
MEM_DQS6P	MEM_DQ29	AE13
MEM_DQS7P	MEM_DQ30	AE12
MEM_DQ31	MEM_DQ31	AE11
MEM_DQ32	MEM_DQ32	AE10
MEM_DQ33	MEM_DQ33	AE9
MEM_DQ34	MEM_DQ34	AE8
MEM_DQ35	MEM_DQ35	AE7
MEM_DQ36	MEM_DQ36	AE6
MEM_DQ37	MEM_DQ37	AE5
MEM_DQ38	MEM_DQ38	AE4
MEM_DQ39	MEM_DQ39	AE3
MEM_DQ40	MEM_DQ40	AE2
MEM_DQ41	MEM_DQ41	AE1
MEM_DQ42	MEM_DQ42	AE0
MEM_DQ43	MEM_DQ43	AE0
MEM_DQ44	MEM_DQ44	AE0
MEM_DQ45	MEM_DQ45	AE0
MEM_DQ46	MEM_DQ46	AE0
MEM_DQ47	MEM_DQ47	AE0
MEM_DQ48	MEM_DQ48	AE0
MEM_DQ49	MEM_DQ49	AE0
MEM_DQ50	MEM_DQ50	AE0
MEM_DQ51	MEM_DQ51	AE0
MEM_DQ52	MEM_DQ52	AE0
MEM_DQ53	MEM_DQ53	AE0
MEM_DQ54	MEM_DQ54	AE0
MEM_DQ55	MEM_DQ55	AE0
MEM_DQ56	MEM_DQ56	AE0
MEM_DQ57	MEM_DQ57	AE0
MEM_DQ58	MEM_DQ58	AE0
MEM_DQ59	MEM_DQ59	AE0
MEM_DQ60	MEM_DQ60	AE0
MEM_DQ61	MEM_DQ61	AE0
MEM_DQ62	MEM_DQ62	AE0
MEM_DQ63	MEM_DQ63	AE0

PART 3 OF 6

MEM_A I/F



NO DVO:
MEM_COMP = NC
MEM_COMPN = NC
MEM_CAP1 = 470nF
MEM_CAP2 = 470nF
MEM_VMODE = GND (IF VDD_MEM = 2.5V)
MEM_VREF = VDD_MEM / 2

WITH DVO:
MEM_COMP = 61.9 OHM TO GND
MEM_COMPN = 61.9 OHM TO VDD_MEM
MEM_CAP1 = NC
MEM_CAP2 = NC
MEM_VMODE = 1.8V (IF VDD_MEM = 1.8V)
MEM_VREF = VDD_MEM / 2

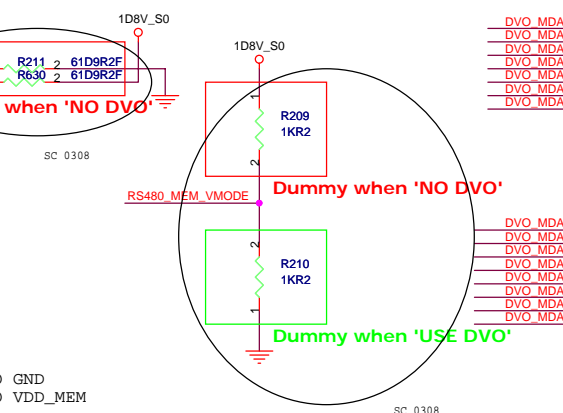
PART 2 OF 6		
PEG_TXP15	D8	GFX_RX0P
PEG_TXN15	D7	GFX_RX0N
PEG_TXP14	D5	GFX_RX1P
PEG_TXN14	D4	GFX_RX1N
PEG_TXP13	F4	GFX_RX2P
PEG_TXN13	F4	GFX_RX2N
PEG_TXP12	G5	GFX_RX3P
PEG_TXN12	G4	GFX_RX3N
PEG_TXP11	H4	GFX_RX4P
PEG_TXN11	J4	GFX_RX4N
PEG_TXP10	H5	GFX_RX5P
PEG_TXN10	H6	GFX_RX5N
PEG_TXP9	G1	GFX_RX6P
PEG_TXN9	G2	GFX_RX6N
PEG_TXP8	K5	GFX_RX7P
PEG_TXN8	K4	GFX_RX7N
PEG_TXP7	L4	GFX_RX8P
PEG_TXN7	M4	GFX_RX8N
PEG_TXP6	N4	GFX_RX9P
PEG_TXN6	N4	GFX_RX9N
PEG_TXP5	P4	GFX_RX10P
PEG_TXN5	R4	GFX_RX10N
PEG_TXP4	P5	GFX_RX11P
PEG_TXN4	P6	GFX_RX11N
PEG_TXP3	P2	GFX_RX12P
PEG_TXN3	R2	GFX_RX12N
PEG_TXP2	T5	GFX_RX13P
PEG_TXN2	T4	GFX_RX13N
PEG_TXP1	U4	GFX_RX14P
PEG_TXN1	V4	GFX_RX14N
PEG_TXP0	W1	GFX_RX15P
PEG_TXN0	W2	GFX_RX15N

LANE REVERSE

PCIE I/F TO VIDEO

GPP_RX0P/SB_RX2P	AE1	GPP_TX0P/SB_TX2P	AD2
GPP_RX0N/SB_RX2N	AE2	GPP_TX0N/SB_TX2N	AD1
GPP_RX1P/SB_RX3P	AB2	GPP_TX1P/SB_TX3P	AA1
GPP_RX1N/SB_RX3N	AB3	GPP_TX1N/SB_TX3N	AB1
GPP_RX2P	AB4	GPP_TX2P	Y5
GPP_RX2N	AB4	GPP_TX2N	Y6
GPP_RX3P	Y4	GPP_TX3P	W5
GPP_RX3N	AA4	GPP_TX3N	W4
SB_RX0P	AG1	SB_TX0P	AF2
SB_RX0N	AH1	SB_TX0N	AG2
SB_RX1P	AC5	SB_TX1P	AC4
SB_RX1N	AC6	SB_TX1N	AD4
PCE_ISET	AE3	PCE_NCAL	AH2
PCE_TXISET	AE3	PCE_NCAL	AJ2

PCIE I/F TO SB



Dummy when 'NO DVO'

Dummy when 'NO DVO'

Dummy when 'USE DVO'

PEG_RXP15 NB	C742	1	2	SCD1U16V	PEG_RXP15
PEG_RXN15 NB	C743	1	2	SCD1U16V	PEG_RXN15
PEG_RXP14 NB	C744	1	2	SCD1U16V	PEG_RXP14
PEG_RXN14 NB	C745	1	2	SCD1U16V	PEG_RXN14
PEG_RXP13 NB	C746	1	2	SCD1U16V	PEG_RXP13
PEG_RXN13 NB	C747	1	2	SCD1U16V	PEG_RXN13
PEG_RXP12 NB	C748	1	2	SCD1U16V	PEG_RXP12
PEG_RXN12 NB	C749	1	2	SCD1U16V	PEG_RXN12
PEG_RXP11 NB	C751	1	2	SCD1U16V	PEG_RXP11
PEG_RXN11 NB	C750	1	2	SCD1U16V	PEG_RXN11
PEG_RXP10 NB	C774	1	2	SCD1U16V	PEG_RXP10
PEG_RXN10 NB	C772	1	2	SCD1U16V	PEG_RXN10
PEG_RXP9 NB	C777	1	2	SCD1U16V	PEG_RXP9
PEG_RXN9 NB	C776	1	2	SCD1U16V	PEG_RXN9
PEG_RXP8 NB	C770	1	2	SCD1U16V	PEG_RXP8
PEG_RXN8 NB	C773	1	2	SCD1U16V	PEG_RXN8
PEG_RXP7 NB	C781	1	2	SCD1U16V	PEG_RXP7
PEG_RXN7 NB	C780	1	2	SCD1U16V	PEG_RXN7
PEG_RXP6 NB	C775	1	2	SCD1U16V	PEG_RXP6
PEG_RXN6 NB	C771	1	2	SCD1U16V	PEG_RXN6
PEG_RXP5 NB	C779	1	2	SCD1U16V	PEG_RXP5
PEG_RXN5 NB	C778	1	2	SCD1U16V	PEG_RXN5
PEG_RXP4 NB	C799	1	2	SCD1U16V	PEG_RXP4
PEG_RXN4 NB	C801	1	2	SCD1U16V	PEG_RXN4
PEG_RXP3 NB	C807	1	2	SCD1U16V	PEG_RXP3
PEG_RXN3 NB	C803	1	2	SCD1U16V	PEG_RXN3
PEG_RXP2 NB	C797	1	2	SCD1U16V	PEG_RXP2
PEG_RXN2 NB	C800	1	2	SCD1U16V	PEG_RXN2
PEG_RXP1 NB	C805	1	2	SCD1U16V	PEG_RXP1
PEG_RXN1 NB	C806	1	2	SCD1U16V	PEG_RXN1
PEG_RXP0 NB	C802	1	2	SCD1U16V	PEG_RXP0
PEG_RXN0 NB	C798	1	2	SCD1U16V	PEG_RXN0

Dummy when use UMA

LANE REVERSE

CHANGE TO 71.RS48M.B0U (VER A22)

DVO_MDA33	DVO_MDA33	15
DVO_MDA34	DVO_MDA34	15
DVO_MDA35	DVO_MDA35	15
DVO_MDA36	DVO_MDA36	15
DVO_MDA37	DVO_MDA37	15
DVO_MDA38	DVO_MDA38	15
DVO_MDA39	DVO_MDA39	15

DVO_MDA48	DVO_MDA48	15
DVO_MDA49	DVO_MDA49	15
DVO_MDA50	DVO_MDA50	15
DVO_MDA51	DVO_MDA51	15
DVO_MDA52	DVO_MDA52	15
DVO_MDA53	DVO_MDA53	15
DVO_MDA54	DVO_MDA54	15
DVO_MDA55	DVO_MDA55	15

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

ATI-RS480M (2 of 4) PCIE

Size

Document Number

Rev

A3

Bolsena

-1

Date:

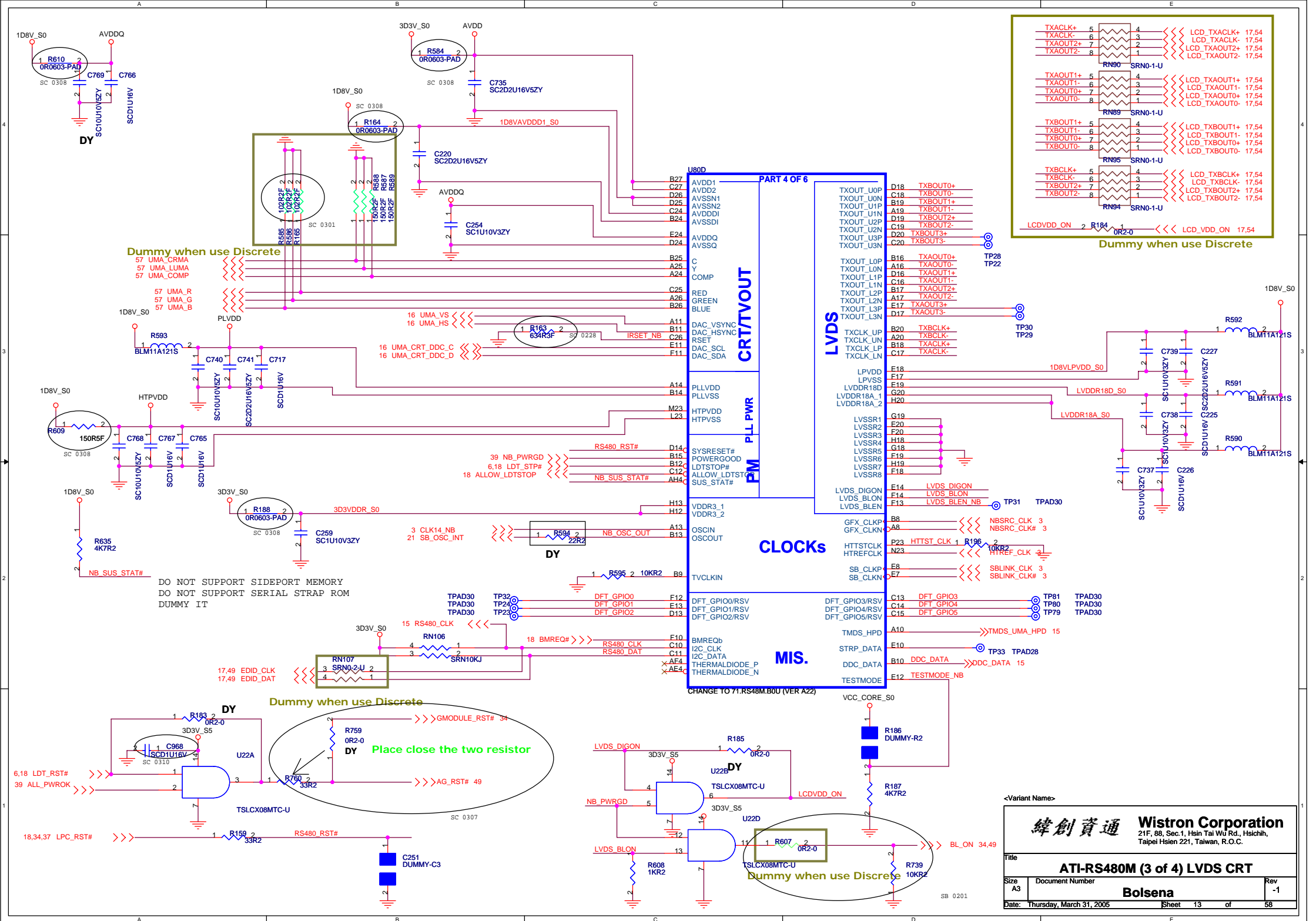
Thursday, March 31, 2005

Sheet

12

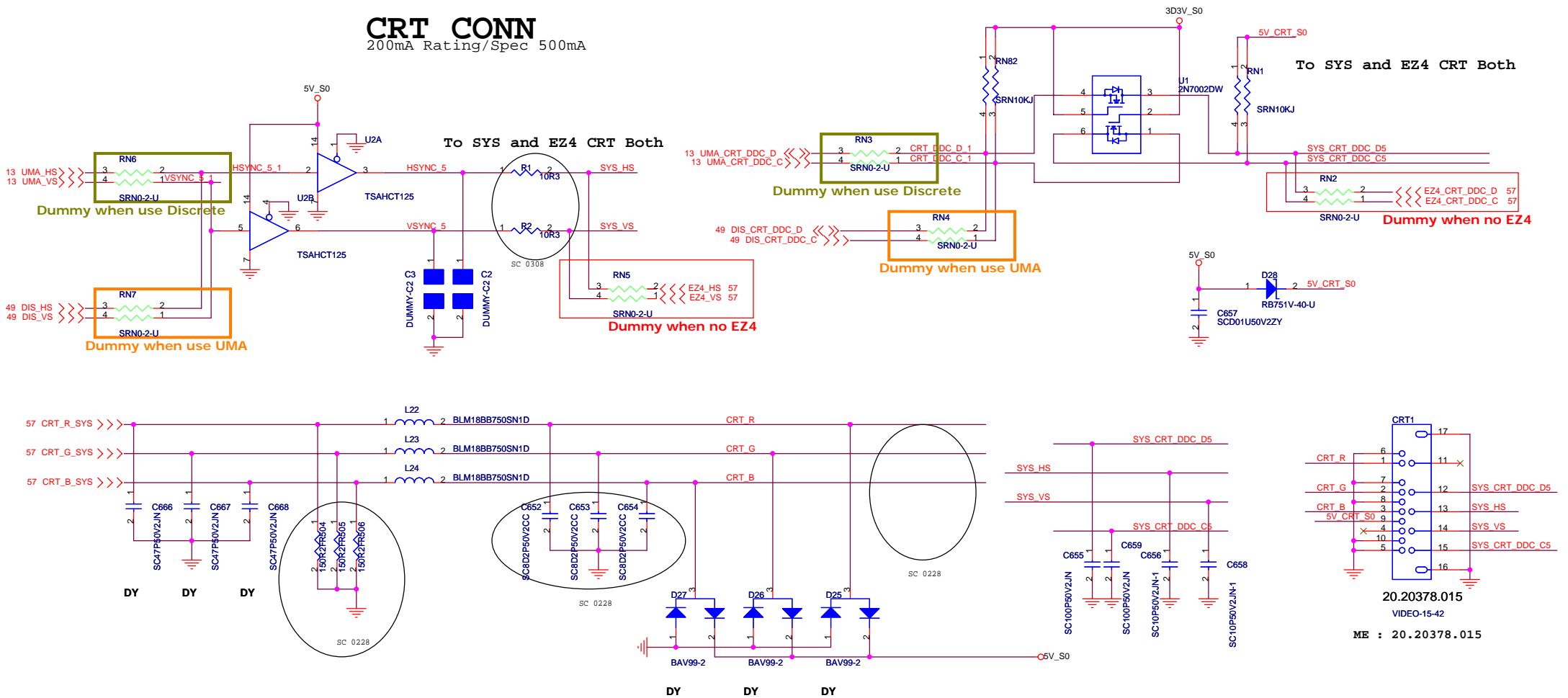
of

58

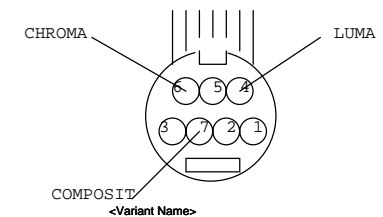
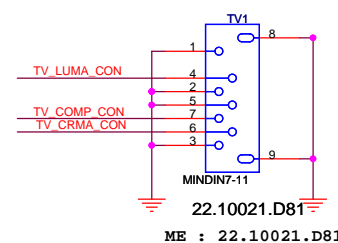
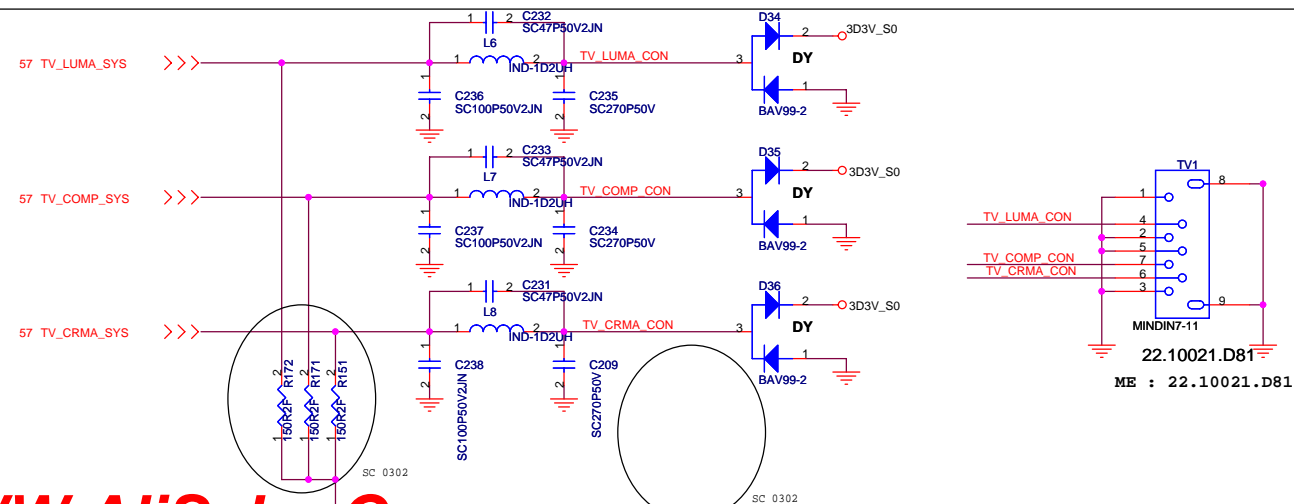




CRT CONN
200mA Rating/Spec 500mA



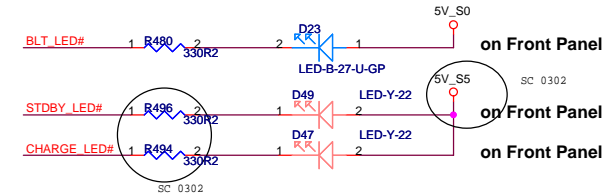
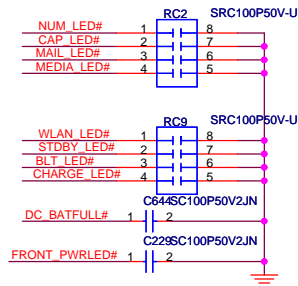
TV CONN



緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
CRT / TV			
Size A3	Document Number		Rev
	Bolsena		-1
Date:	Thursday, March 31, 2005	Sheet 16 of	58

```
?modify R
?half light
```



LED	V	V			V	V	V
Button	V	V	V	V	V		
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM
							HDD

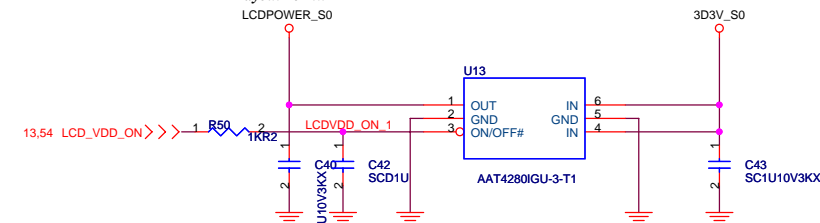
LED	V	V	V	V
Button	V	V		
	Bluetooth	Wireless	Charger	Power2

Power2:
Green : S0
Orange : S3
Orange Blinking : Enter S4

LCD CONN

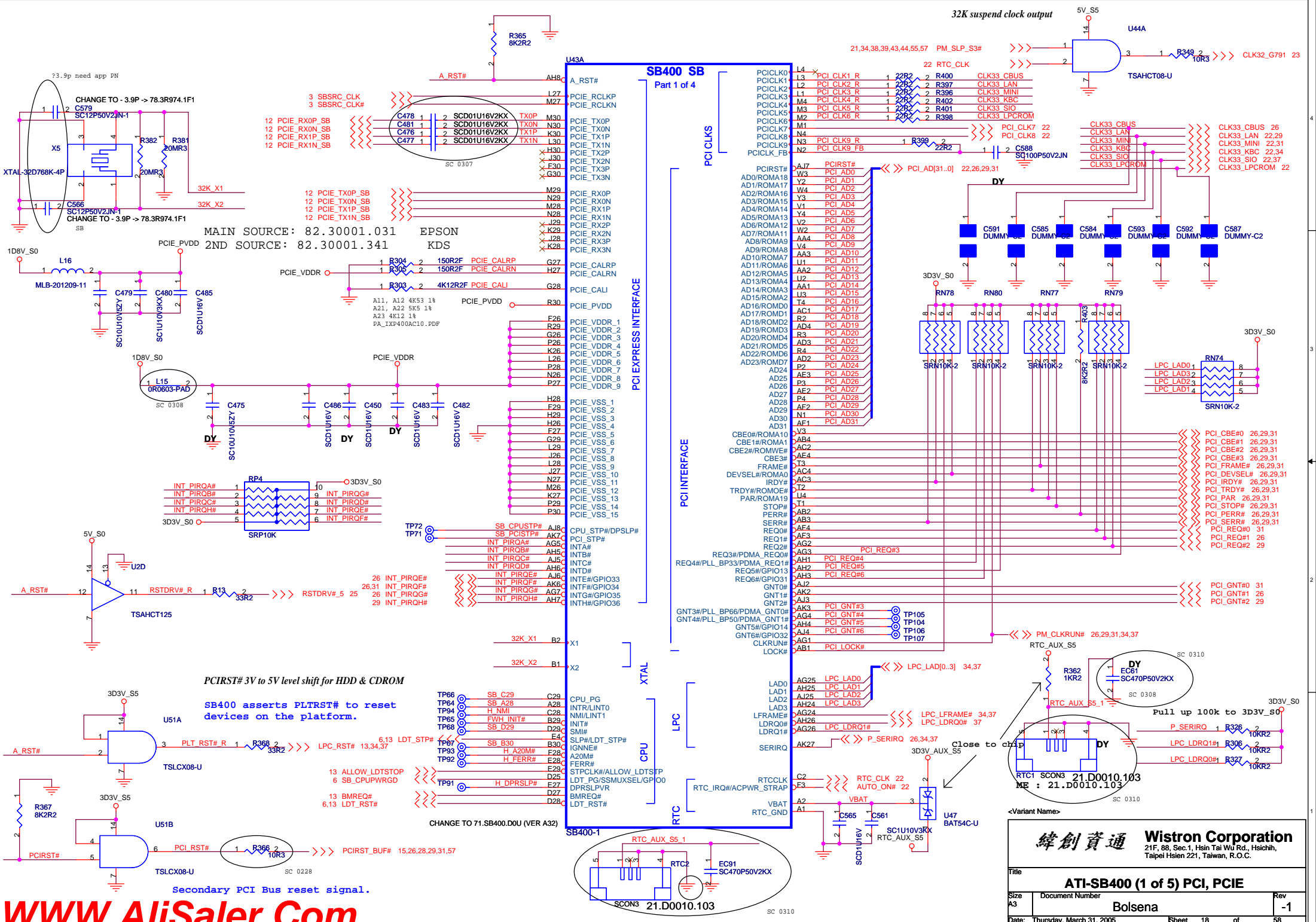


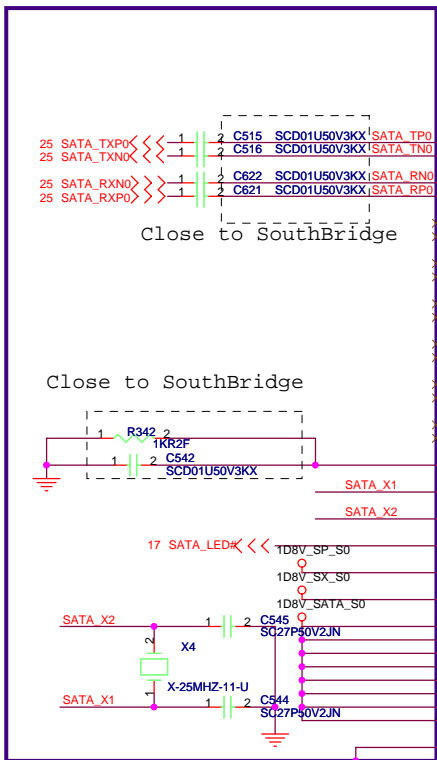
Layout 40 mil
LCDPOWER_S0



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Title			
LCD / LEDs			
Size A3	Document Number		Rev
	Bolsena		-1
Date:	Thursday, March 31, 2005	Sheet 17 of	58





SB400 SB Part 2 of 4

SERIAL ATA

SERIAL ATA POWER

PRIMARY ATA 66/100

SECONDARY ATA 66/100

PIDE_IORDY# AD30
PIDE_IRQ# AE28
PIDE_A0 AD27
PIDE_A1 AC27
PIDE_A2 AD28
PIDE_DACK# AD29
PIDE_DRQ# AE27
PIDE_IOR# AE30
PIDE_IOW# AE29
PIDE_CS1# AC28
PIDE_CS3# AC29

SIDE_IORDY# V29
SIDE_IRQ# T27
SIDE_A0 T28
SIDE_A1 U29
SIDE_A2 T29
SIDE_DACK# V30
SIDE_DRQ# U28
SIDE_IOR# W29
SIDE_IOW# W30
SIDE_CS1# R27
SIDE_CS3# R28

SIDE_D0/GPIO15 V28
SIDE_D1/GPIO16 W28
SIDE_D2/GPIO17 Y30
SIDE_D3/GPIO18 AA30
SIDE_D4/GPIO19 AA28
SIDE_D5/GPIO20 AB28
SIDE_D6/GPIO21 AB27
SIDE_D7/GPIO22 AB29
SIDE_D8/GPIO23 AA27
SIDE_D9/GPIO24 AA29
SIDE_D10/GPIO25 AA29
SIDE_D11/GPIO26 W27
SIDE_D12/GPIO27 V29
SIDE_D13/GPIO28 V27
SIDE_D14/GPIO29 U27
SIDE_D15/GPIO30 U27

AVSS_SATA_33 AG13
AVSS_SATA_34 AH22
AVSS_SATA_35 AK12
AVSS_SATA_36 AH11
AVSS_SATA_37 AJ17
AVSS_SATA_38 AH14
AVSS_SATA_39 AH19
AVSS_SATA_40 AJ20
AVSS_SATA_41 AH21
AVSS_SATA_42 AJ9
AVSS_SATA_43 AG16
AVSS_SATA_44 AK15
AVSS_SATA_45 AK20

SC 0308

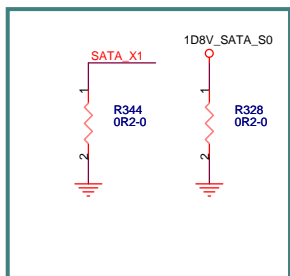
R463 0R0402-PAD
PIDE_DACK# 25
PIDE_A0 25
PIDE_A1 25
PIDE_A2 25
PIDE_DREQ 25
PIDE_IOR# 25
PIDE_IOW# 25
PIDE_CS#0 25
PIDE_CS#1 25

also strap function

PIDE_D[15..0] 25

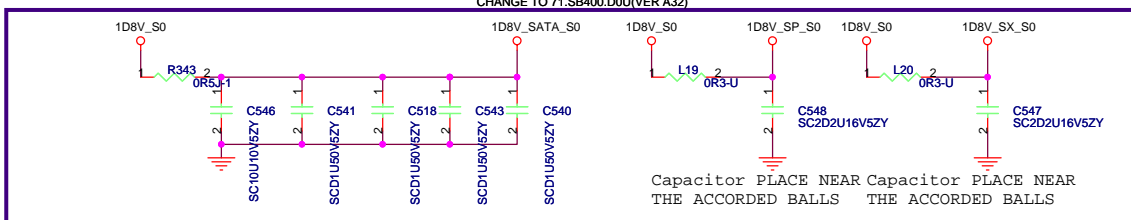
SIDE_D[15..0] 25

Dummy when use IDE



Dummy when use SATA

SB400-1
CHANGE TO 71.SB400.D0U(VER A32)

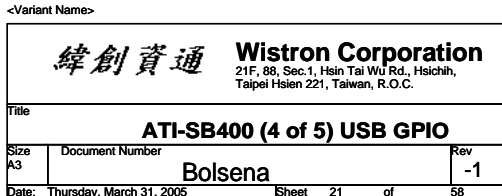


Dummy when use IDE

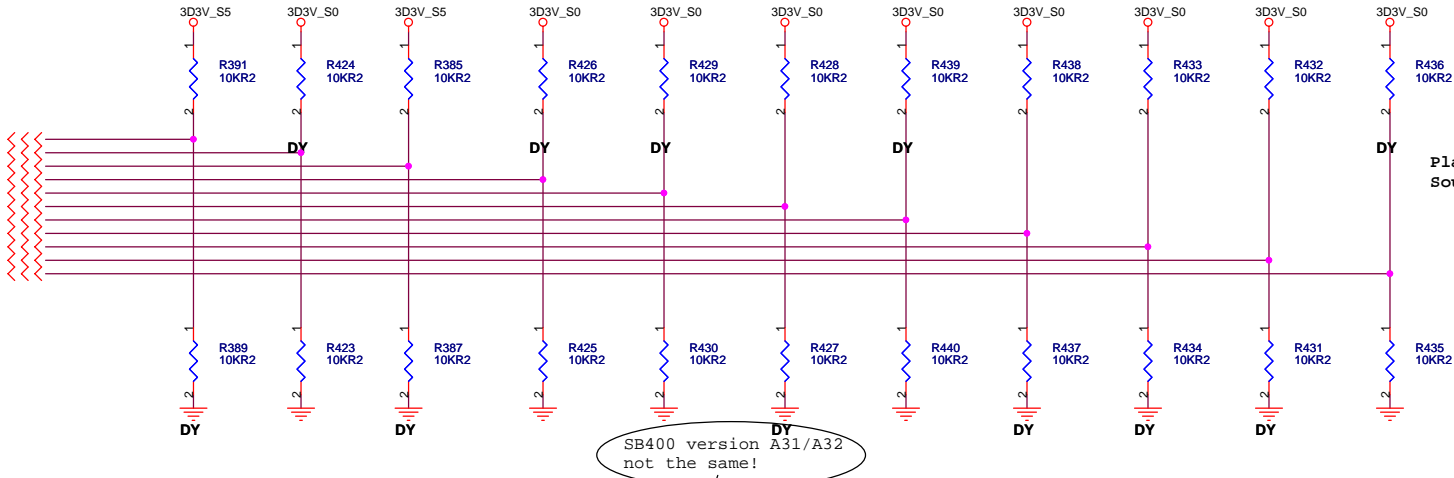
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Size	Document Number	Rev	
A3	Bolsena	-1	
Date:	Thursday, March 31, 2005	Sheet	19 of 58



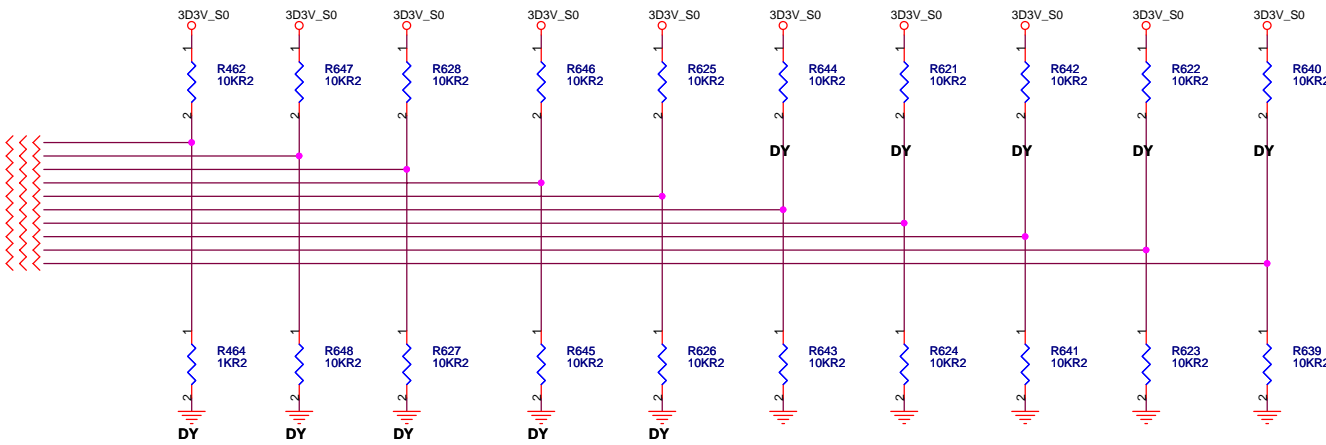
18 AUTO_ON#
21,24,32 AC97_DOUT
18 RTC_CLK
21 SPDIF_OUT_STRAP
18,29 CLK33_LAN
18,31 CLK33_MINI
18,34 CLK33_KBC
18,37 CLK33_SIO
18 CLK33_LPCROM
18 PCI_CLK7
18 PCI_CLK8



REQUIRED SYSTEM STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8
STRAP HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz	48MHZ- Clock Input Buffer	USB PHY PWRDOWN DISABLE	USB INT PLL48	14MHZ OSC MODE	CPU I/F=K8	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I	
	DEFAULT		DEFAULT		DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz	48MHZ -Crysstal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM	
		DEFAULT		DEFAULT							

19 PDACK#
18,26,29,31 PCI_AD31
18,26,29,31 PCI_AD30
18,26,29,31 PCI_AD29
18,26,29,31 PCI_AD28
18,26,29,31 PCI_AD27
18,26,29,31 PCI_AD26
18,26,29,31 PCI_AD25
18,26,29,31 PCI_AD24
18,26,29,31 PCI_AD23



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

Variant Name:

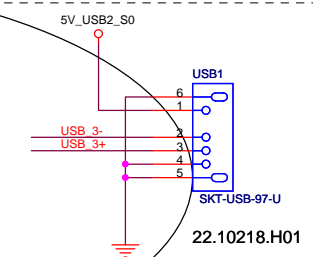
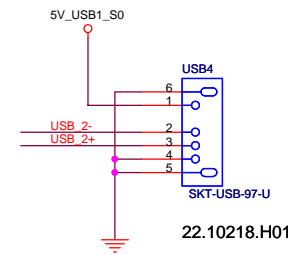
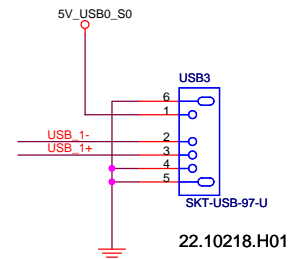
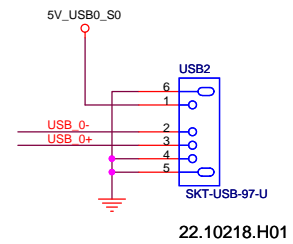
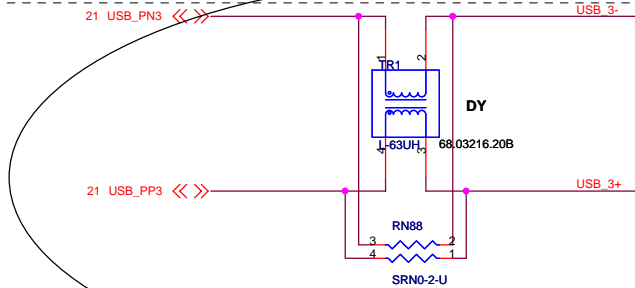
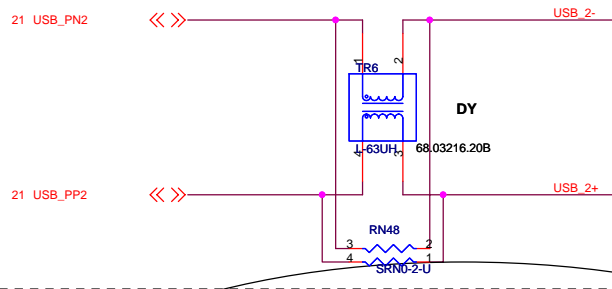
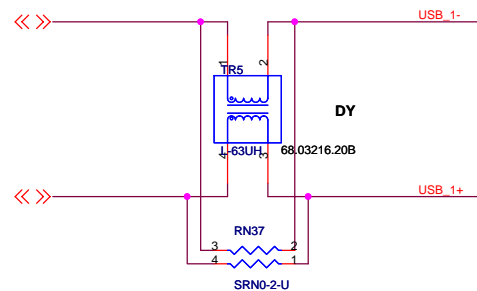
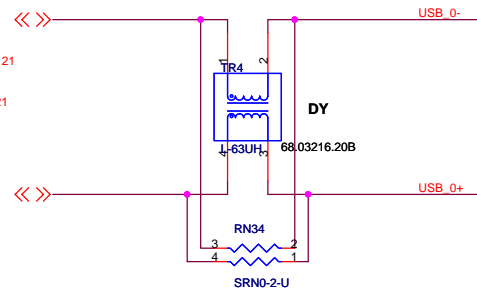
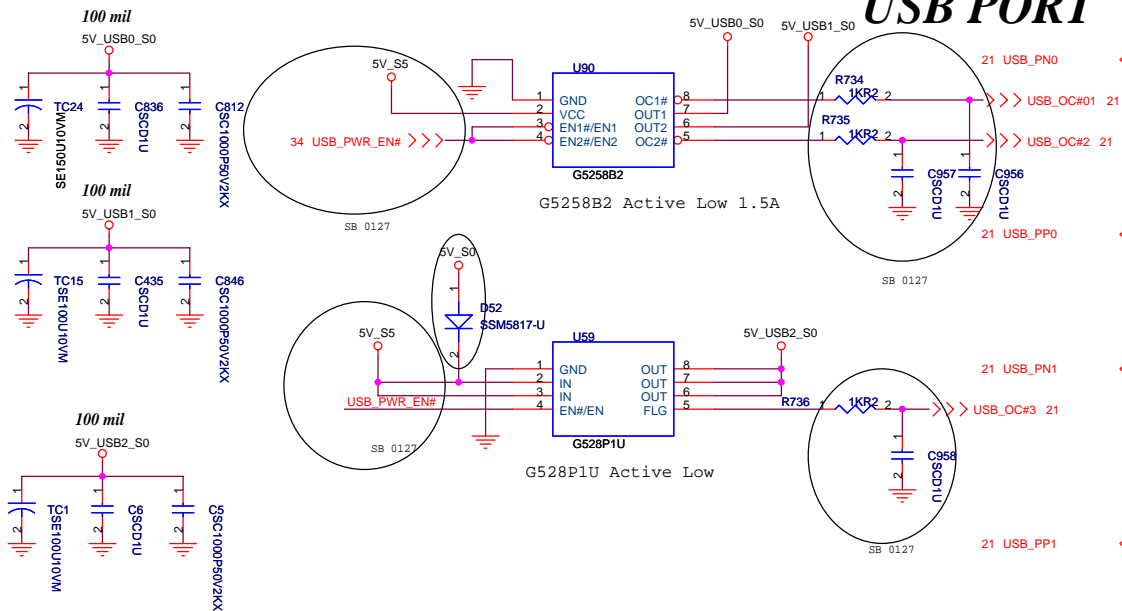
緯創資通 Wistron Corporation
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File: ATI-SB400 STRAPPING(5 of 5)

Size A3 Document Number Bolsena Rev -1

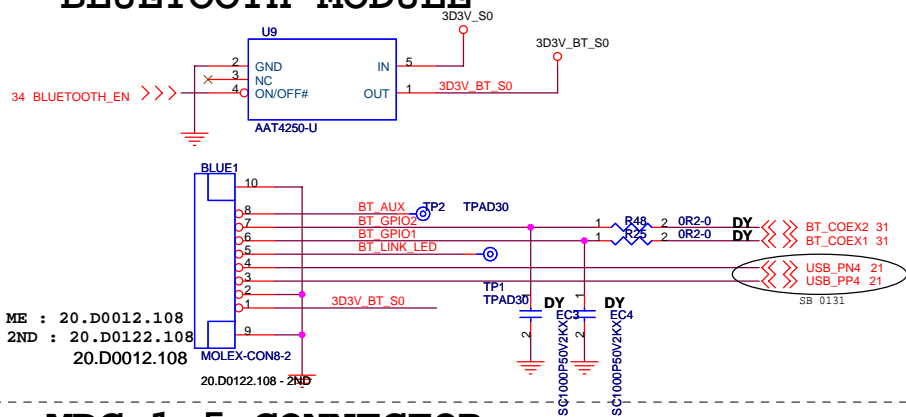
Date: Thursday, March 31, 2005 Sheet 22 of 58

USB PORT

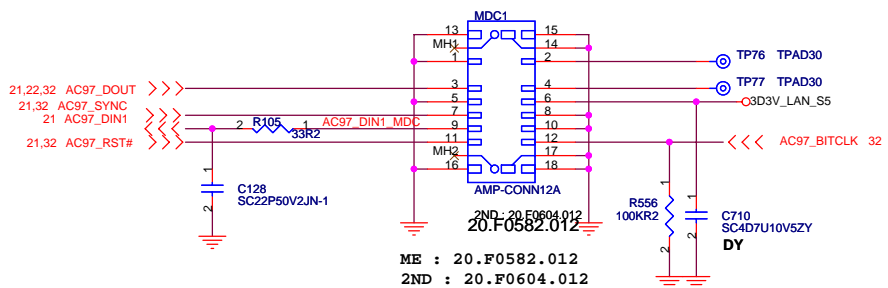


ME : 22.10218.H01
2ND : 22.10218.C91

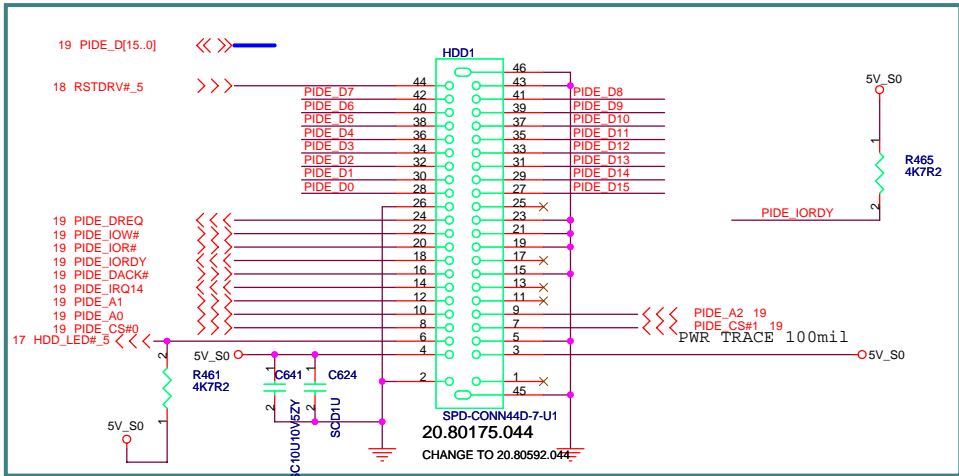
BLUETOOTH MODULE



MDC 1.5 CONNECTOR



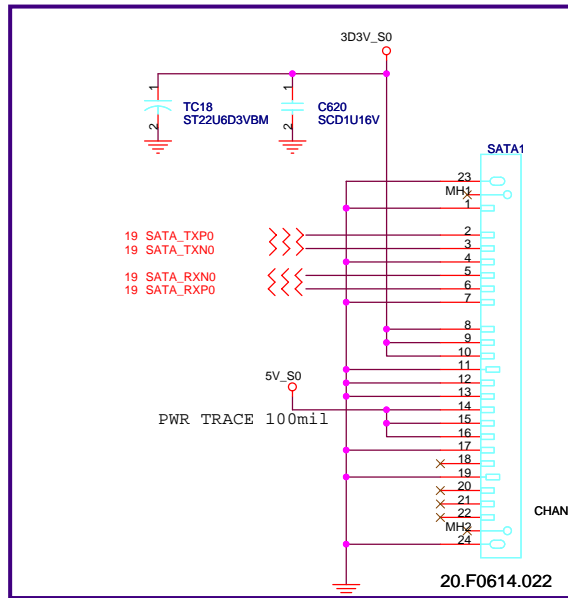
HDD



ME : 20.80592.044
(DIFFERENT FROM ORCAD P/N)

Dummy when use SATA

SATA Connector

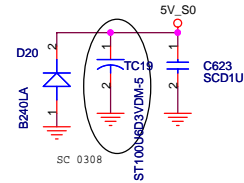


CHANGE TO 20.F0665.022

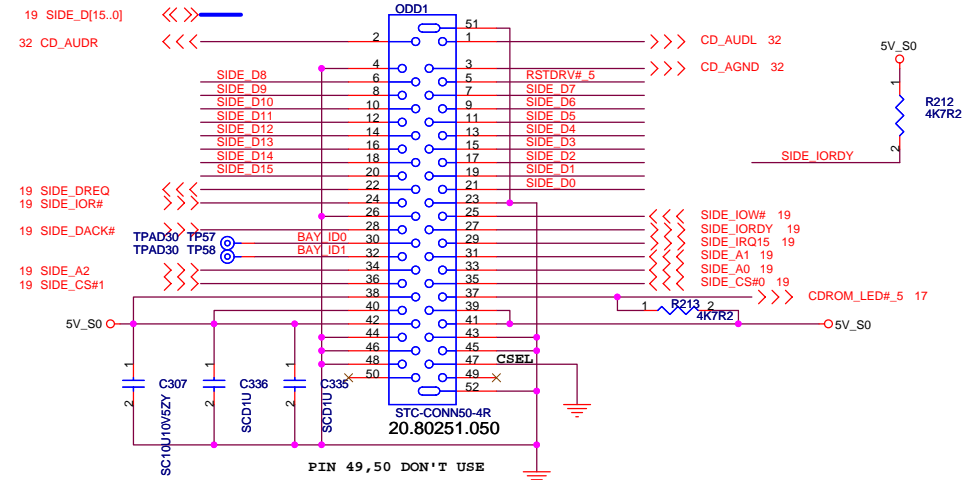
ME : 20.F0665.022
(DIFFERENT FROM ORCAD P/N)

Dummy when use IDE

For HDD & SATA both



CDROM

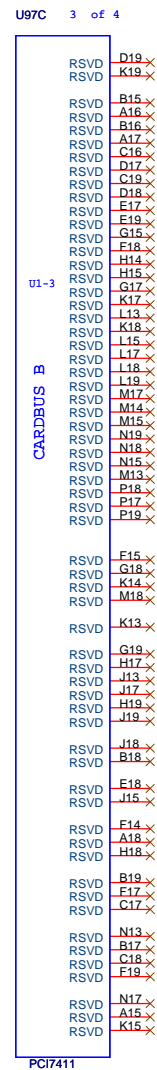


ME : 20.80251.050

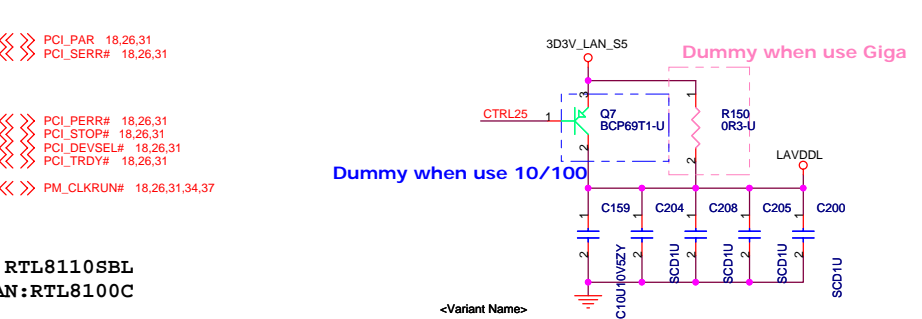
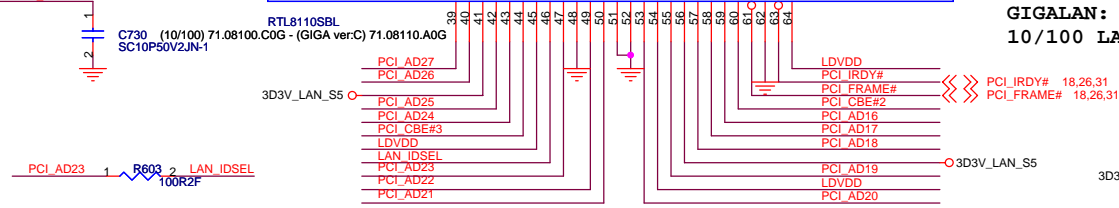
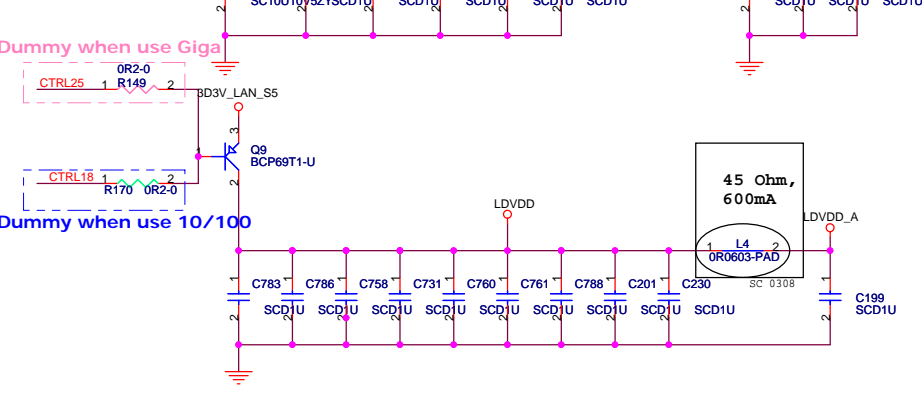
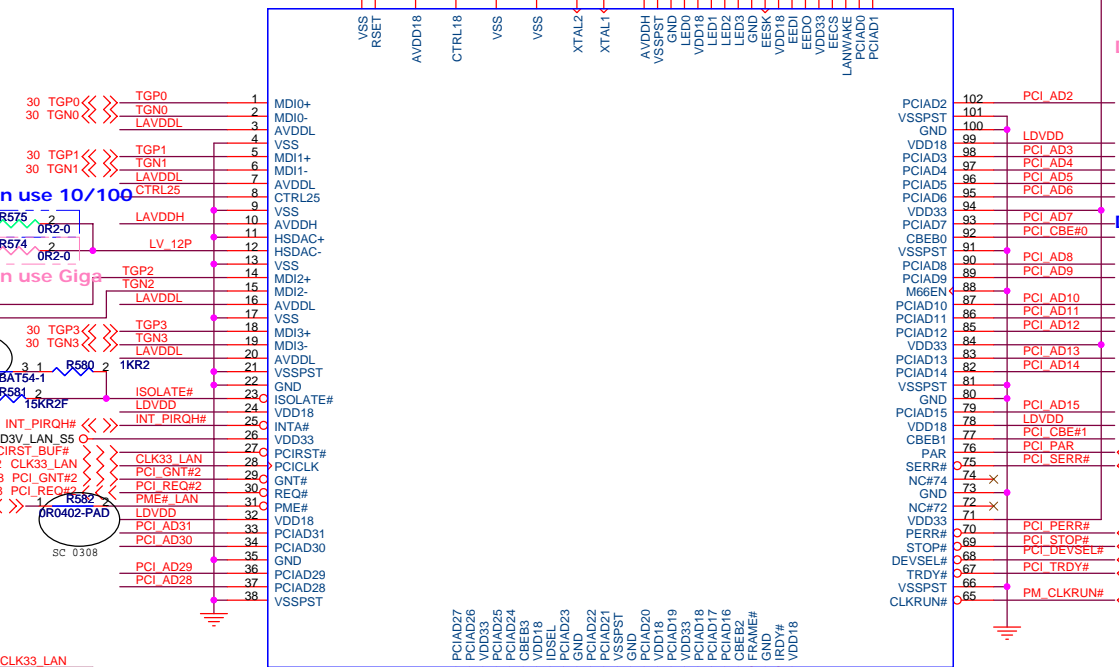
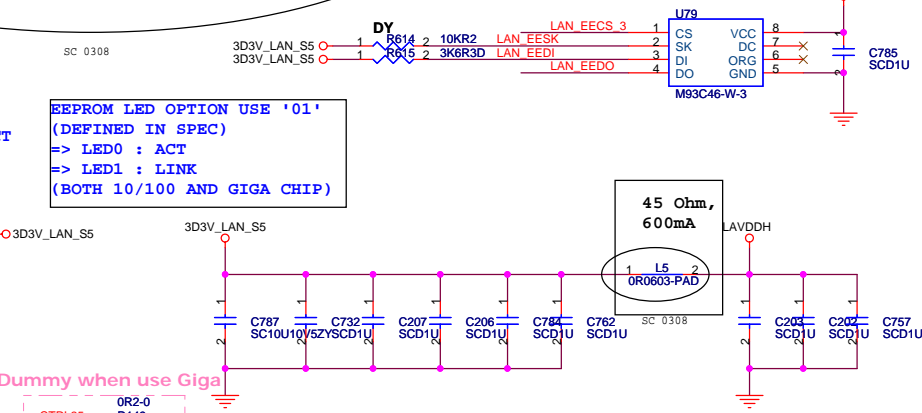
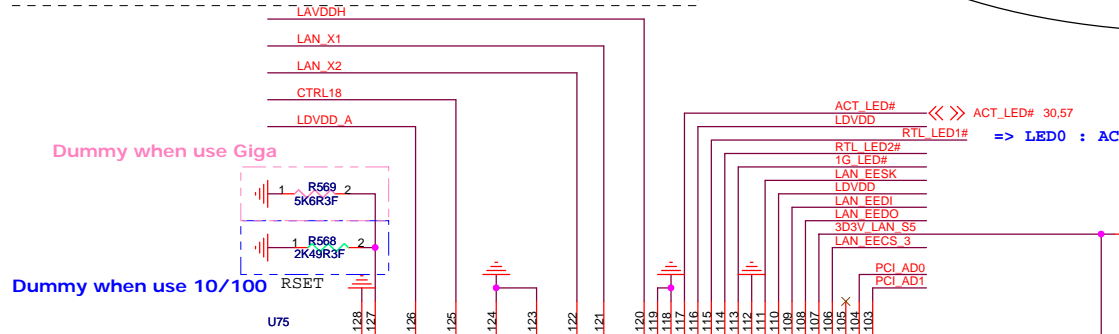
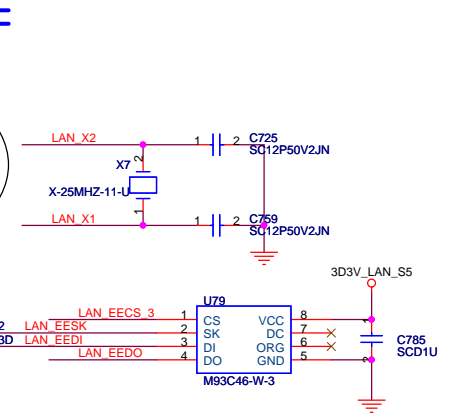
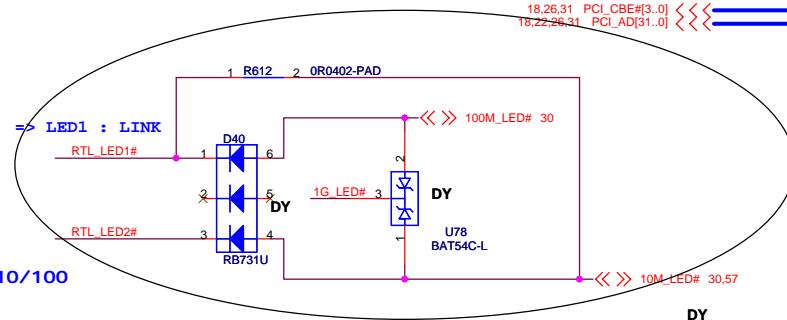
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title		
HDD / CDROM / SATA		
Size	Document Number	Rev
A3	Bolsena	-1
Date: Thursday, March 31, 2005		
Sheet 25 of 58		

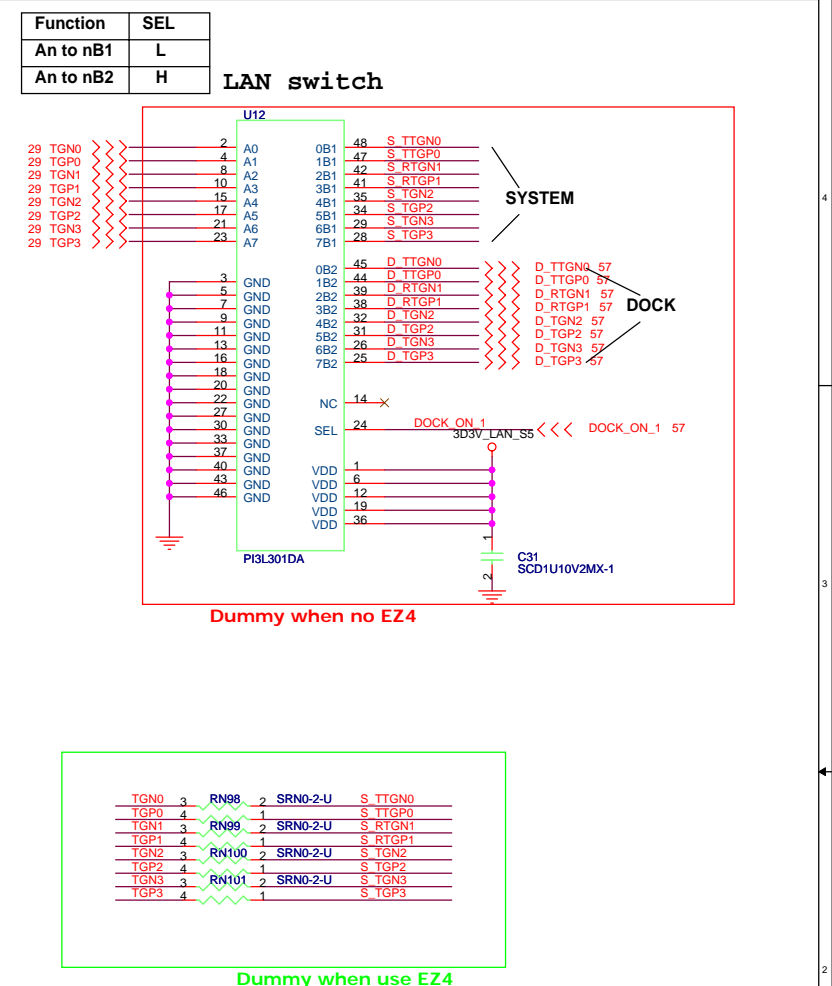
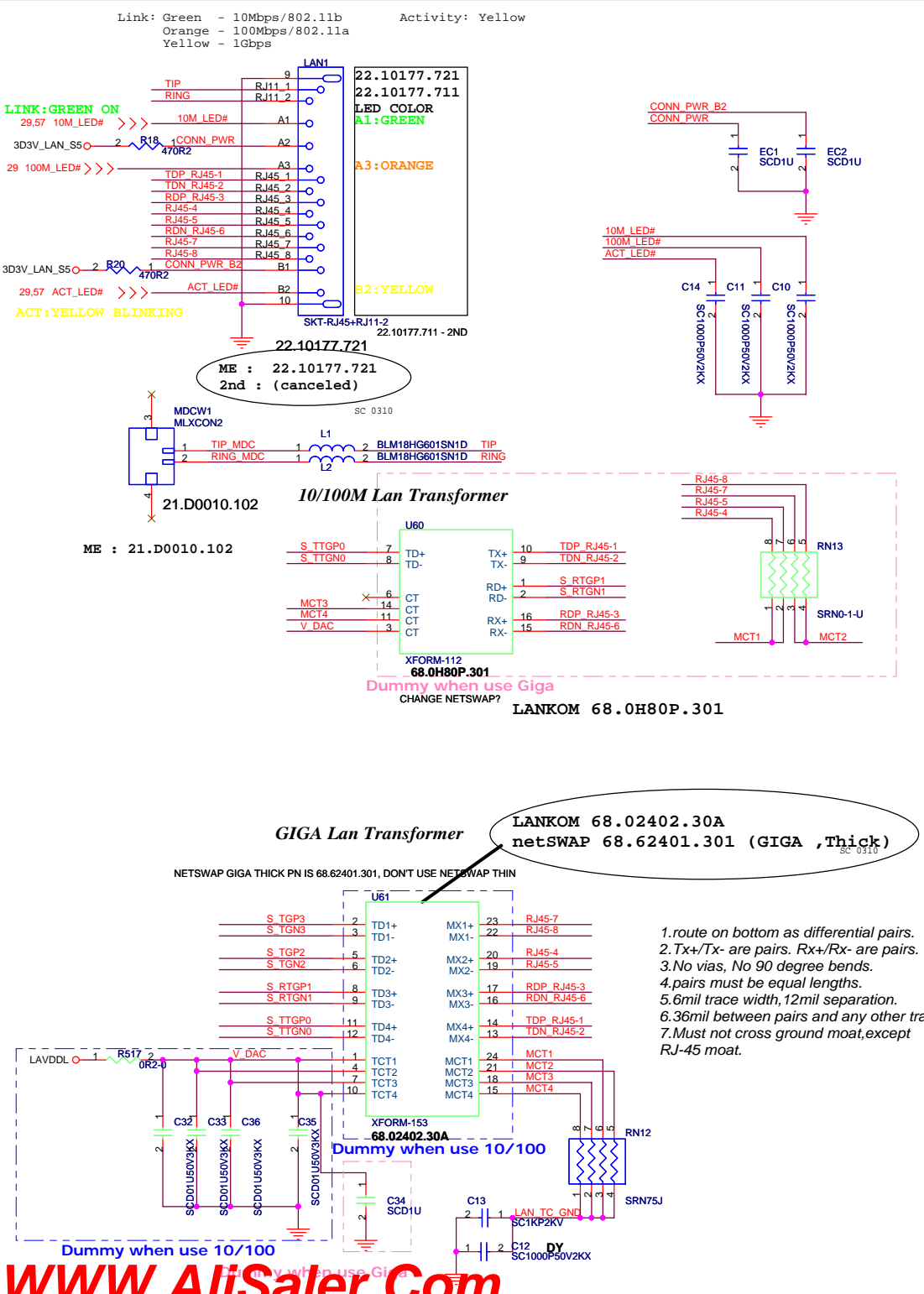


Title			
TI_PCI7411(2 of 2)			
Size A3	Document Number		Rev -1
Bolsena			
Date: Thursday, March 31, 2005	Sheet 27	of 58	

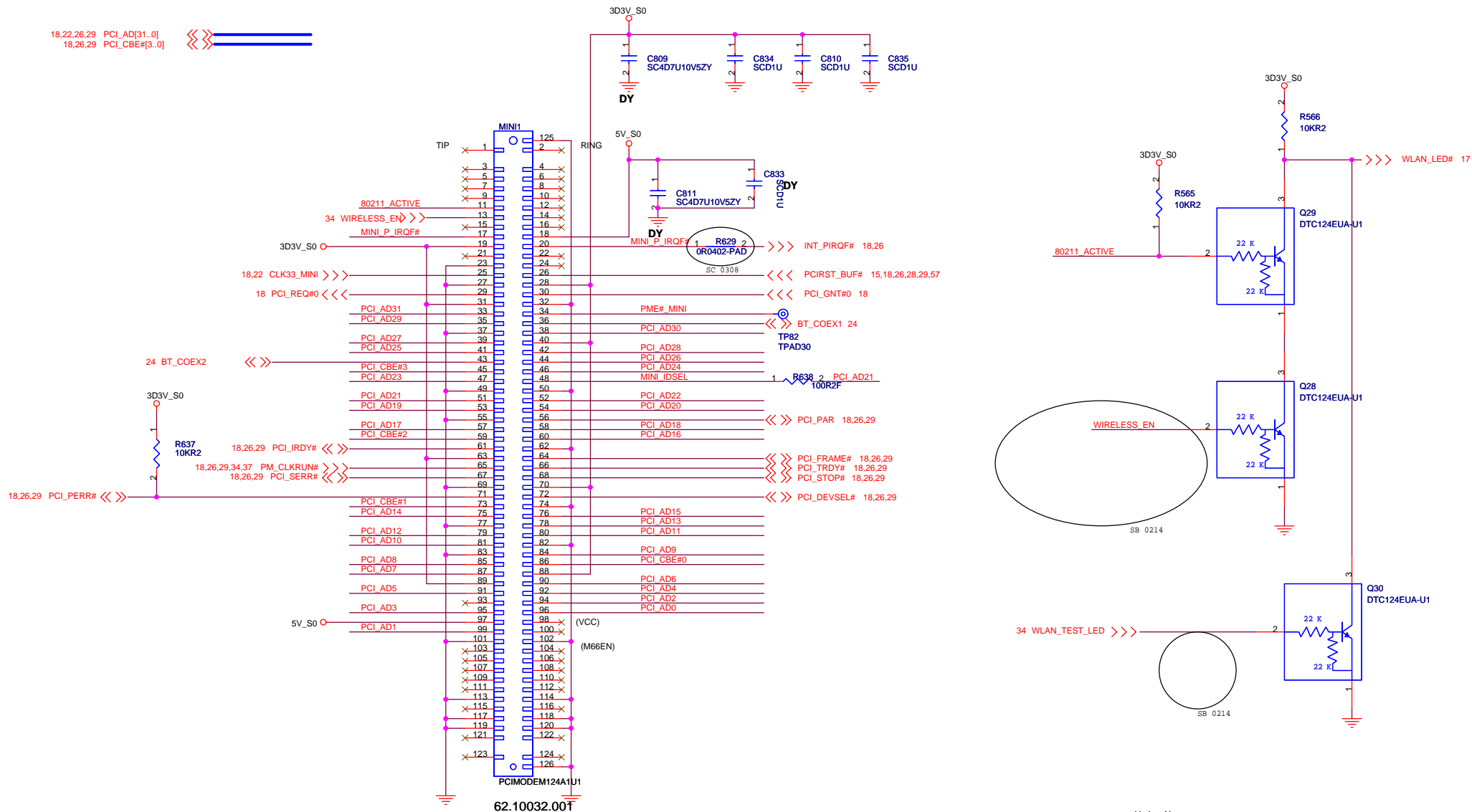


GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C

<Variant Name>		 		\$C10
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title				
RTL8110SBL/RTL8100C				
Size A3	Document Number			Rev -1
Bolsena				
Date:	Thursday, March 31, 2005	Sheet	29 of	58



MINI-PCI



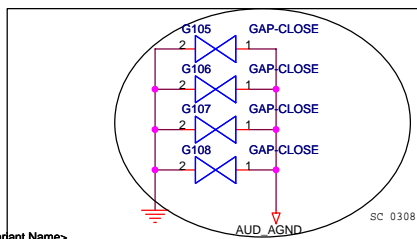
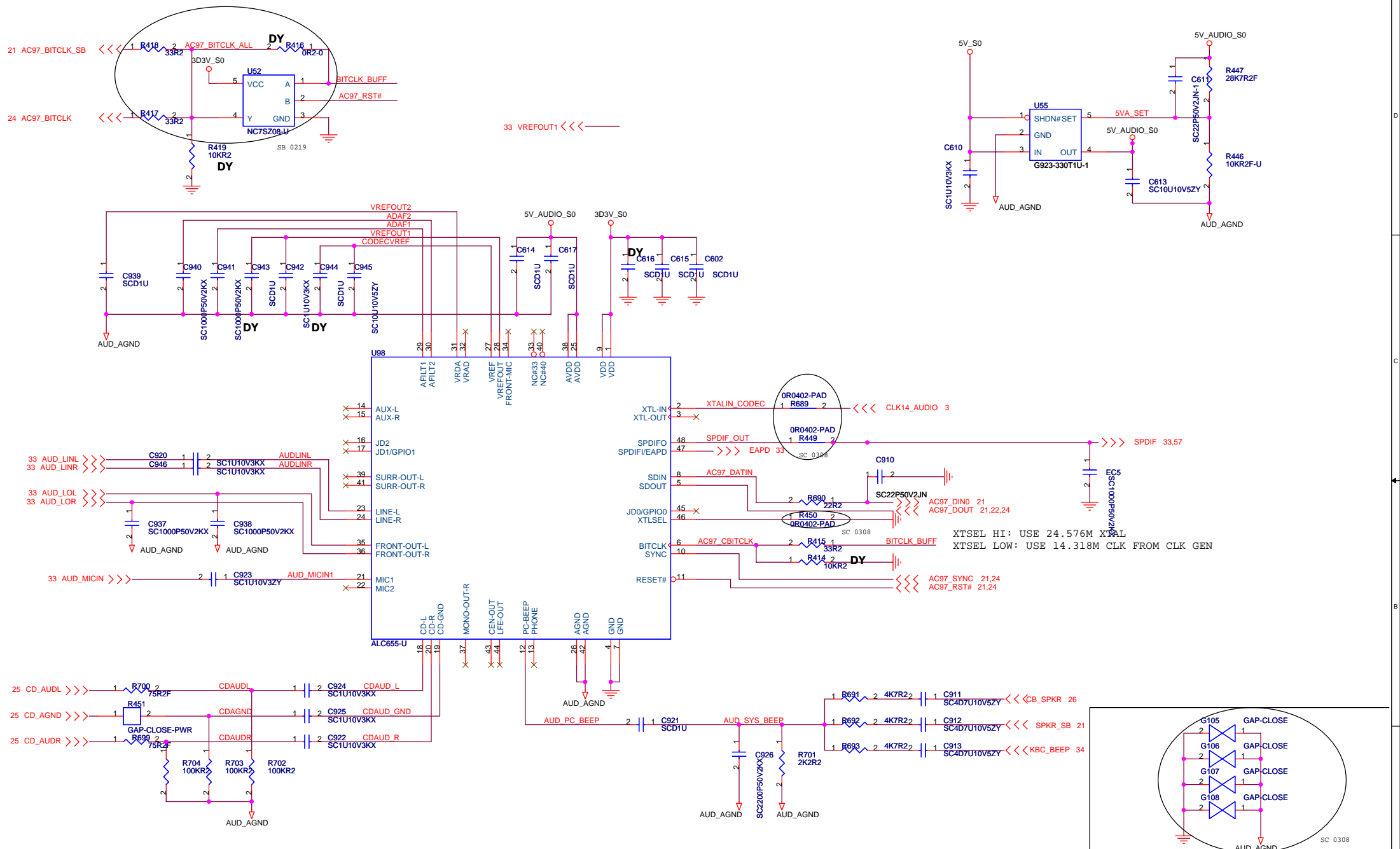
ME : 62.10032.001
2ND : 62.10032.031

62.10032.031 - 2ND

Title		Size		Date	
MINI-PCI		A3		Thursday, March 31, 2005	
Document Number		Sheet		31 of 58	
Bolsena					
Rev		-1			

<Variant Name>

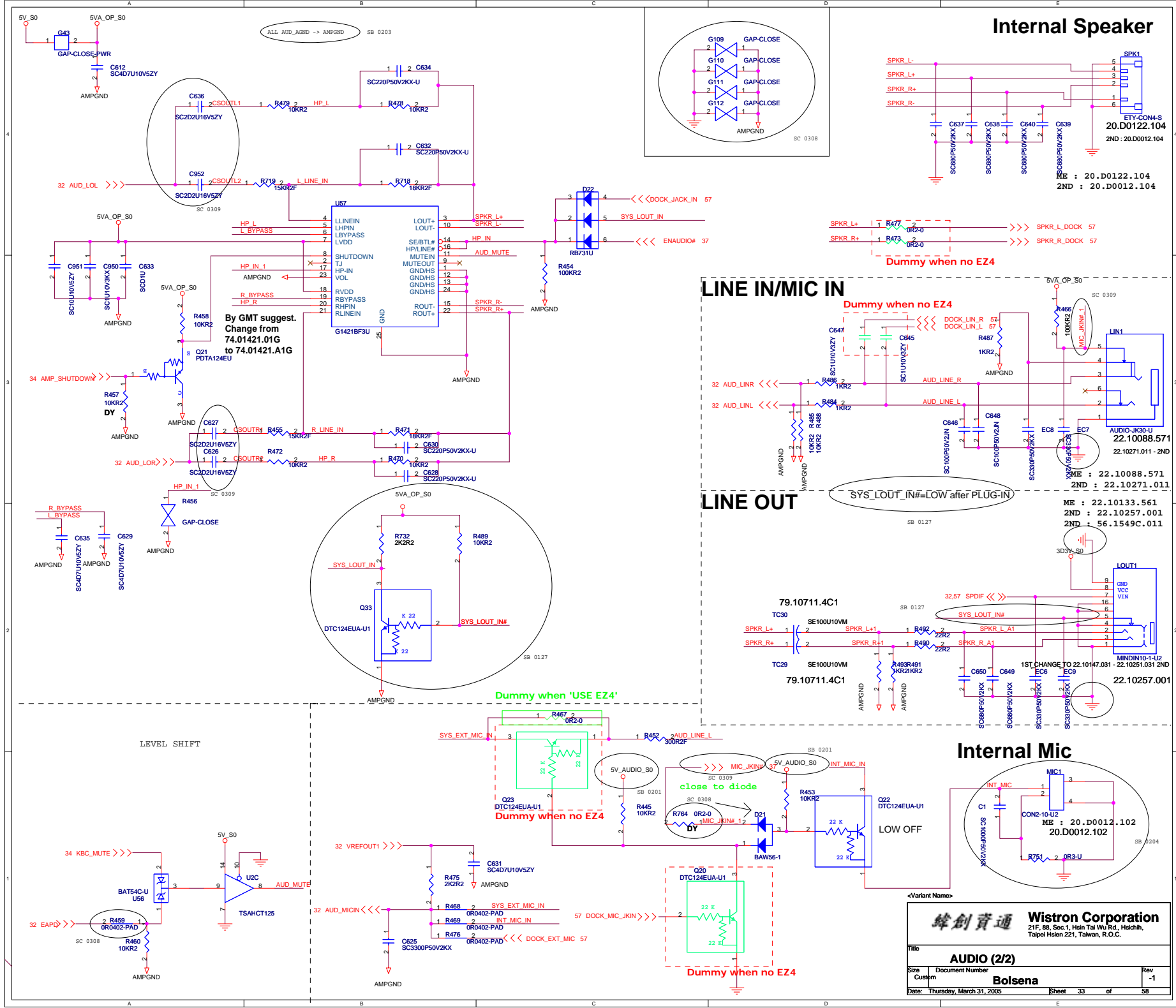
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



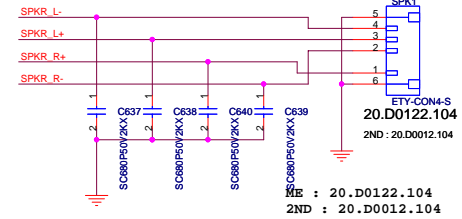
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

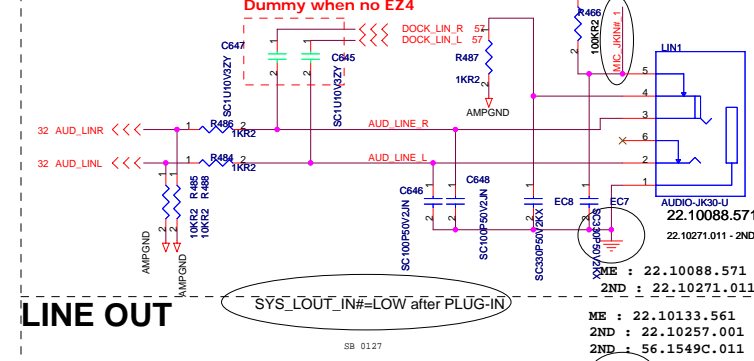
Title			AUDIO (1/2) -- CODEC ALC655	
Size	Document Number			Rev
A3	Bolsena			-1
Date: Thursday, March 31, 2005		Sheet	32	of 58



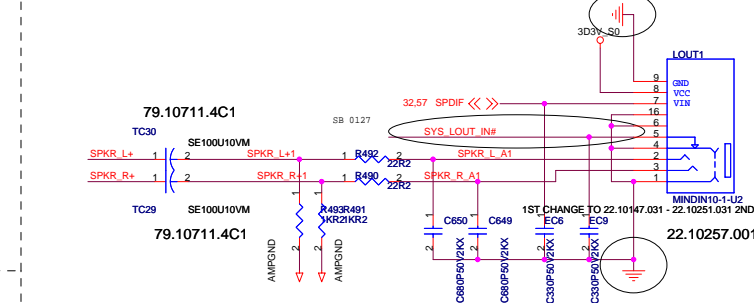
Internal Speaker



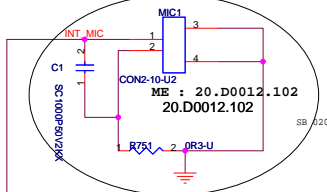
LINE IN/MIC IN



LINE OUT



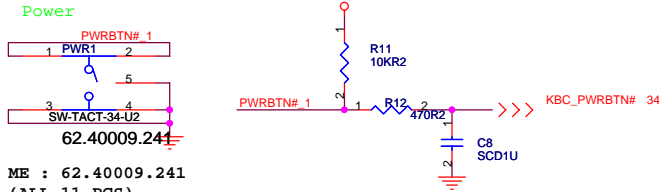
Internal Mic



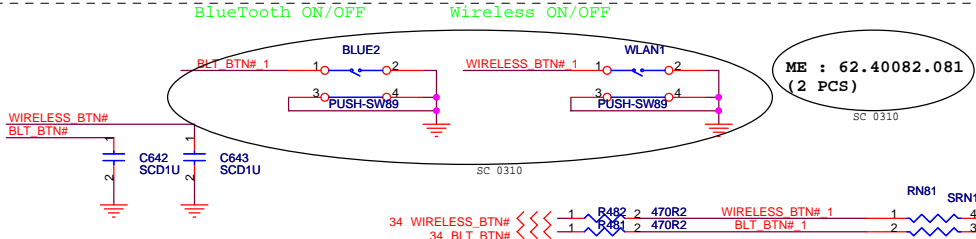
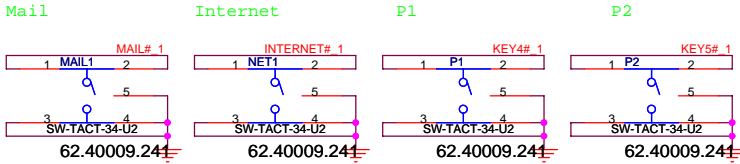
Title			
AUDIO (2/2)			
Size	Document Number	Rev	
Custom	Bolsena	-1	
Date:	Thursday, March 31, 2005	Sheet	33 of 58



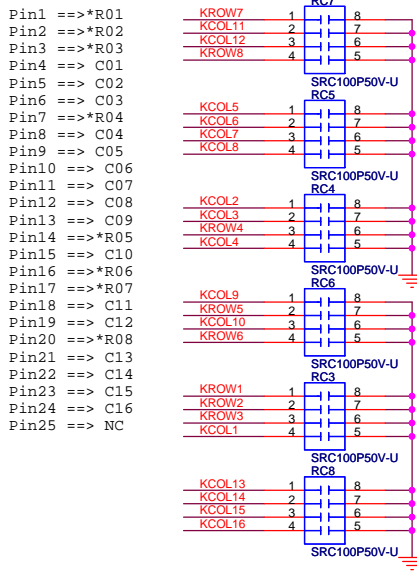
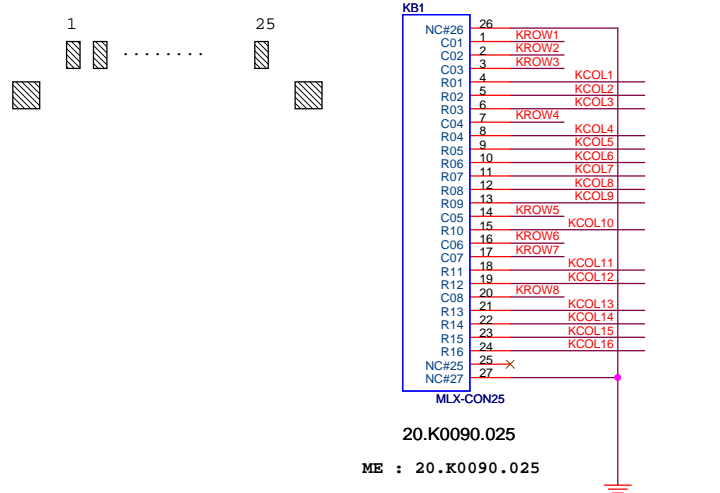
POWER BUTTON



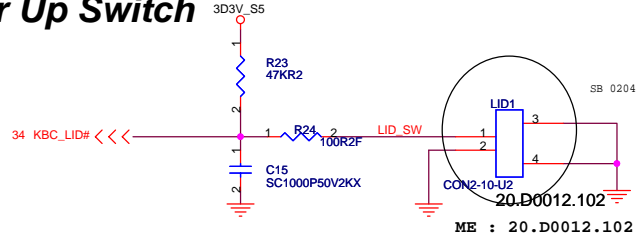
Buttons



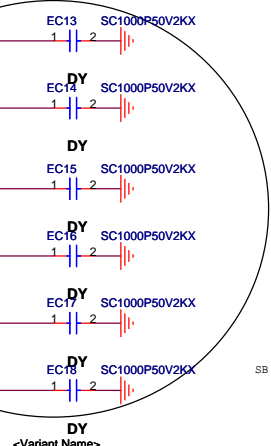
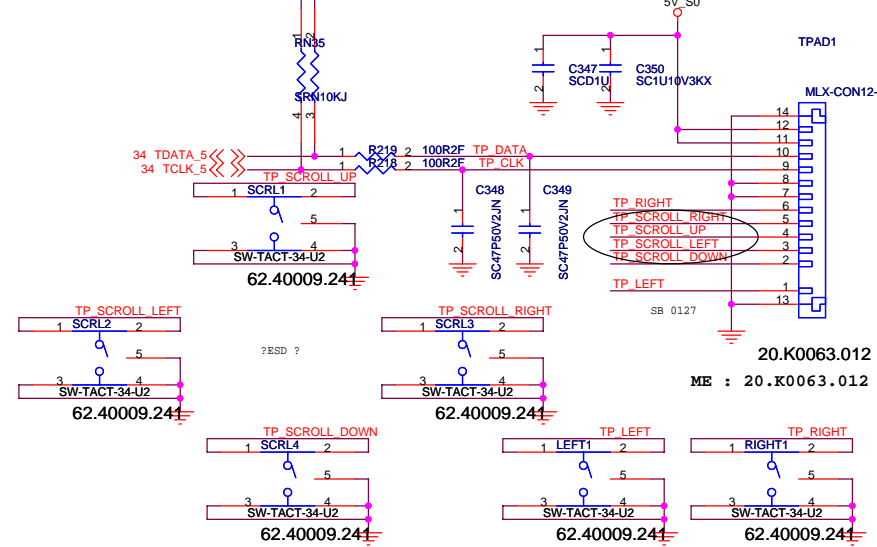
Internal KeyBoard CONN

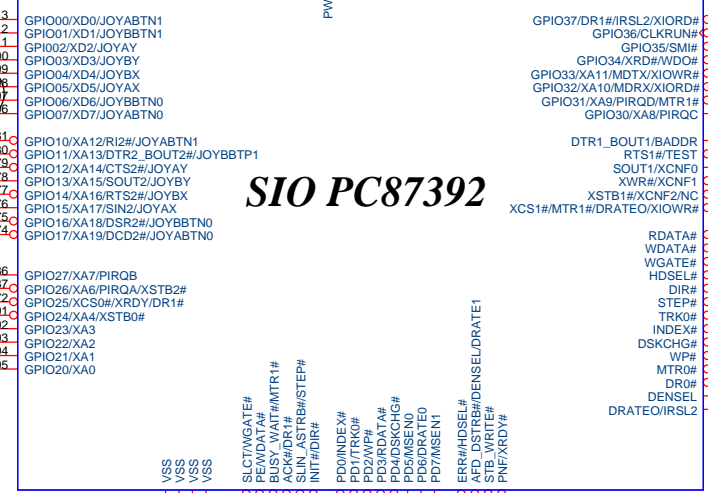
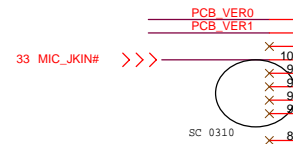
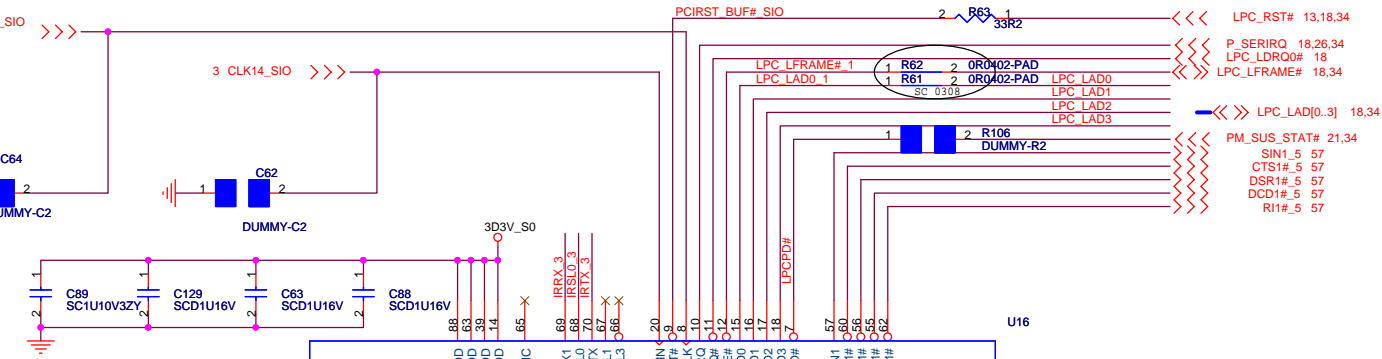
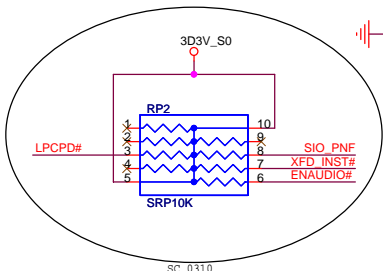


Cover Up Switch



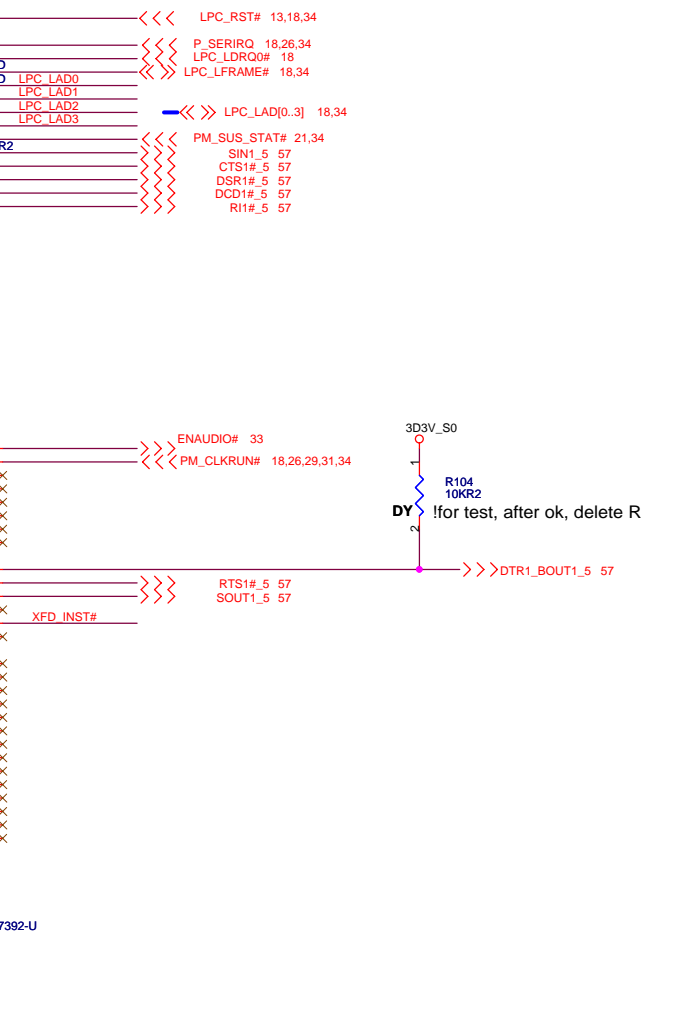
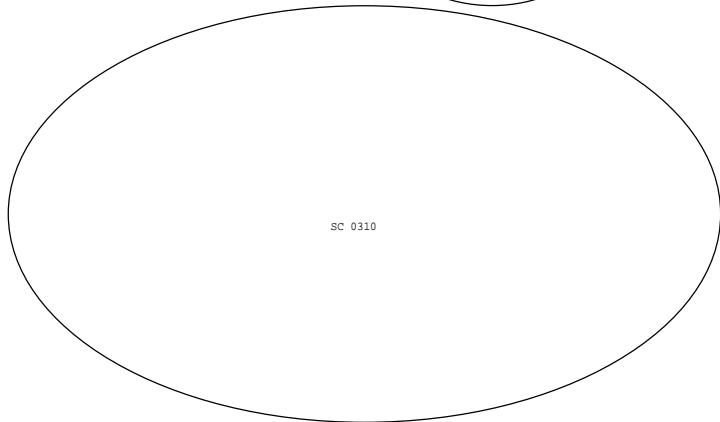
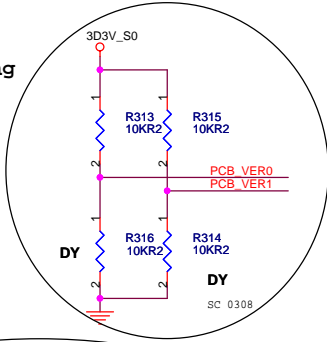
TOUCH PAD





Board Version Setting

Ver.	PCB_VER0	PCB_VER1
SA	0	0
SB	0	1
SC	1	0
1	1	1



Infineon FIR Module

IR1

VCC2/IRED_ANODE

IRED_CATHODE

TXD

RXD

SD

VCC1

MODE

GND

FIR-TF0102

3D3V_S0

C860 SC1U10V3KX

C864 SC4D7U10V5ZY

R67 10KR2

DY

40mil

10mil IRTX_3

10mil IRRX_3

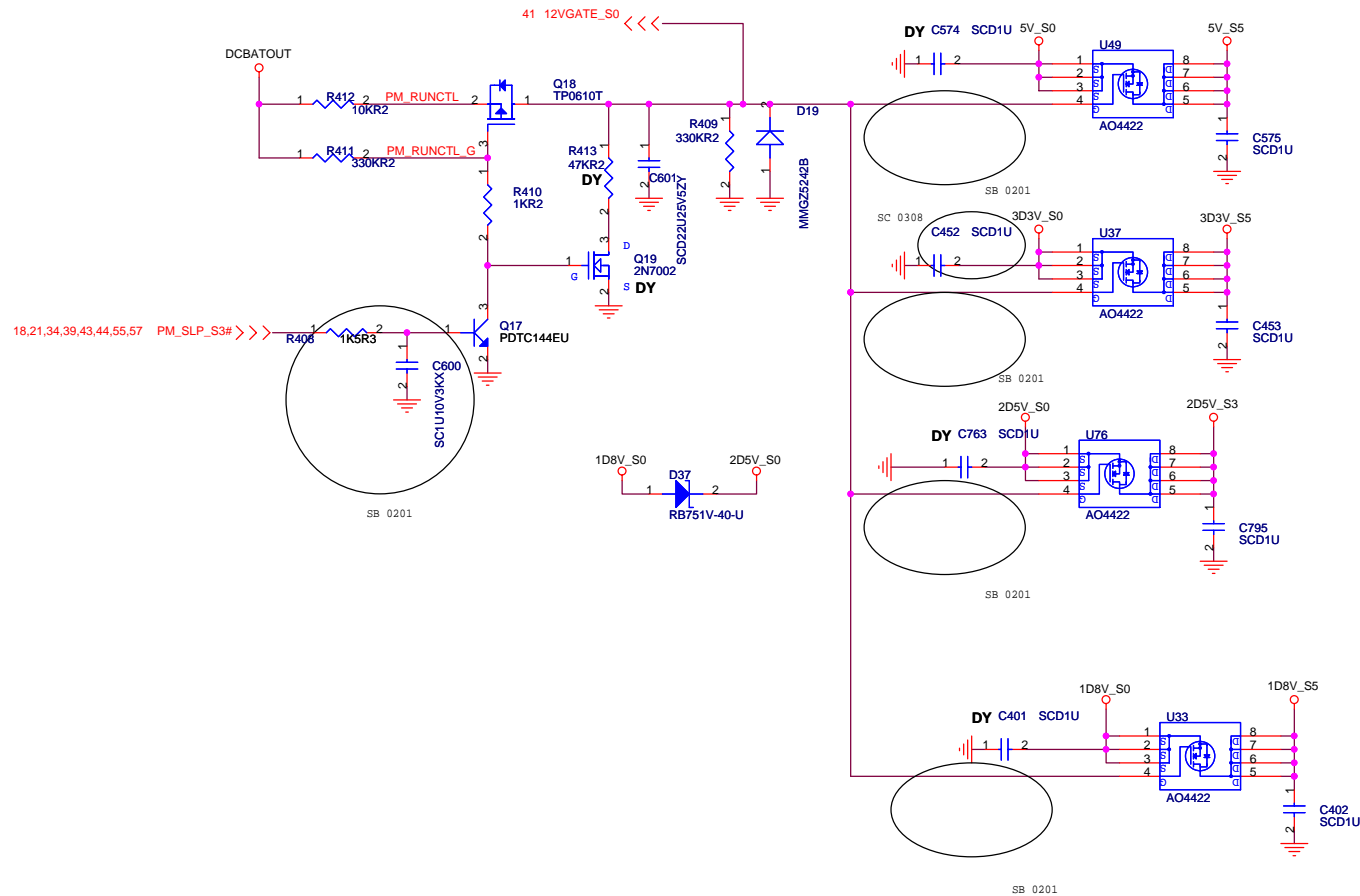
10mil IRRLO_3

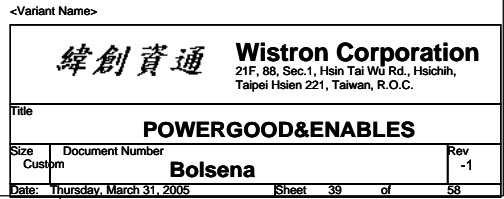
IRMODE

Variant Name>

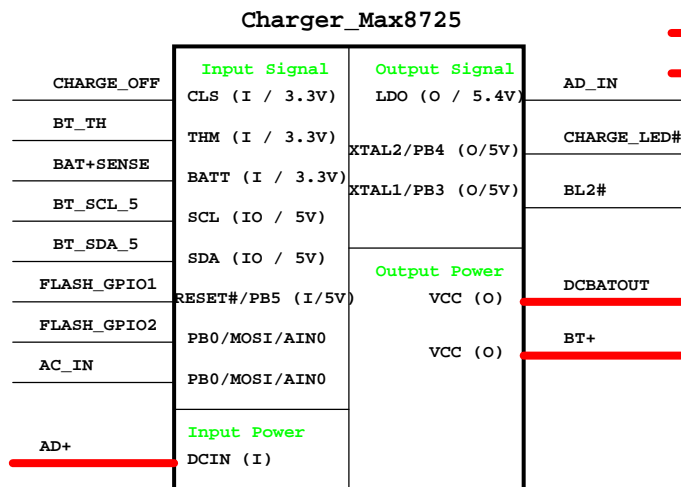
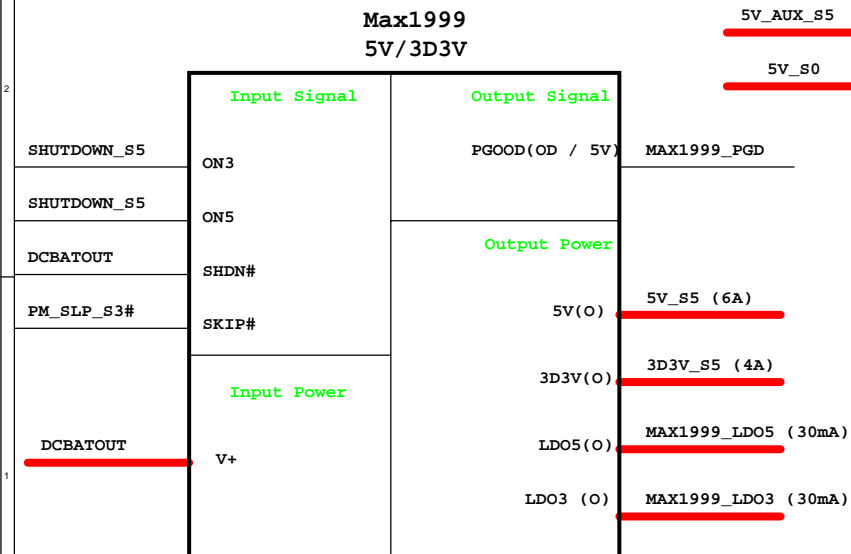
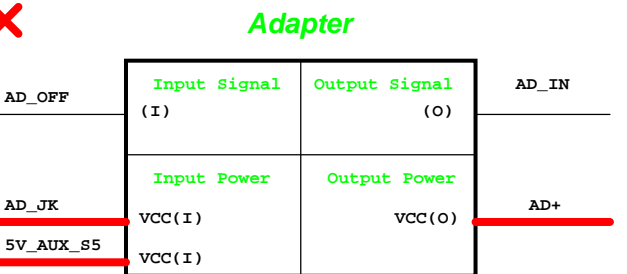
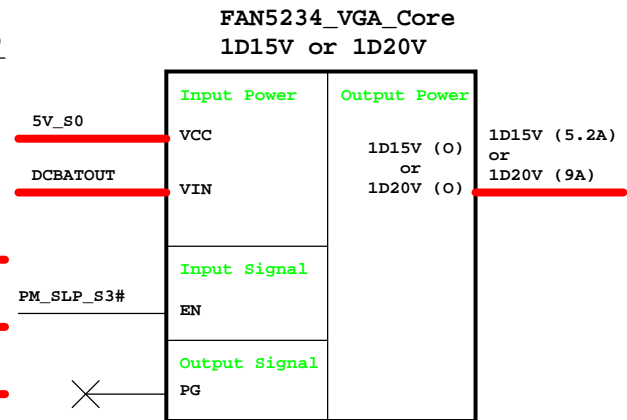
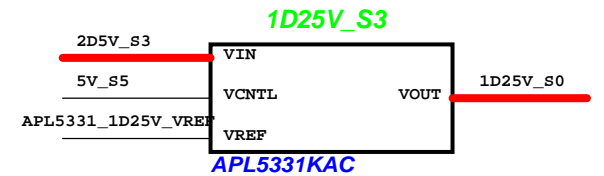
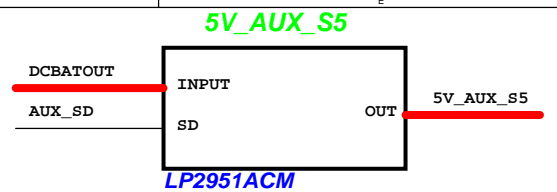
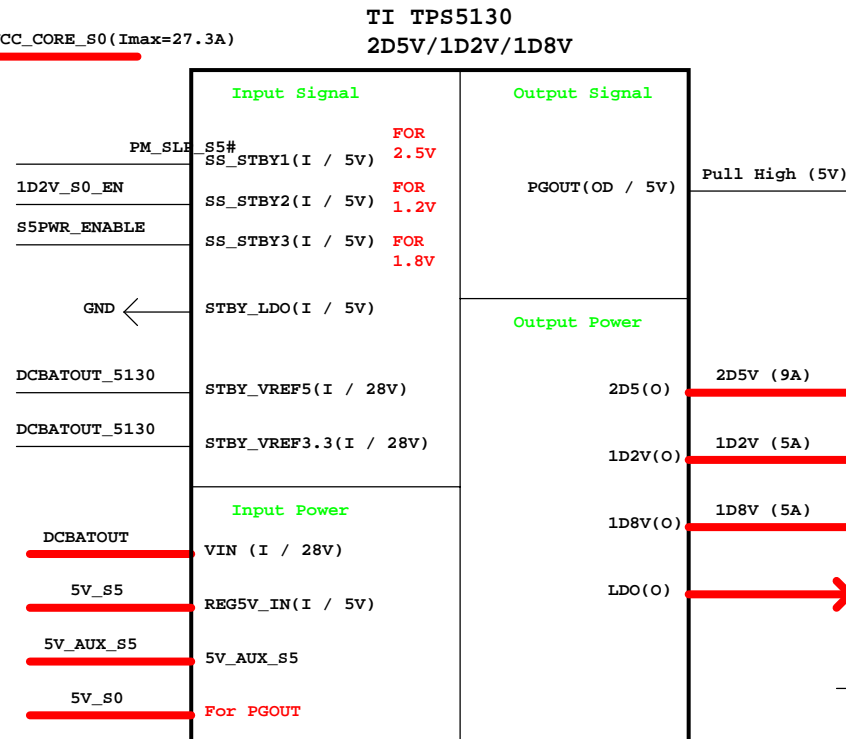
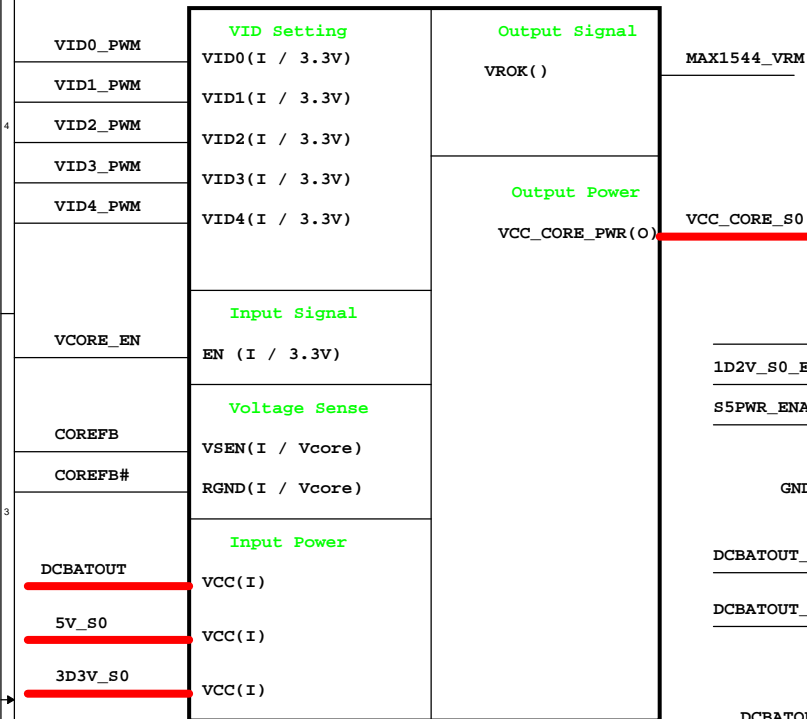
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title SUPER IO NC87392		
Size A3	Document Number Bolsena	Rev -1
Date: Thursday, March 31, 2005	Sheet 37	of 58

Run Power





CPU_CORE MAX1544ETL

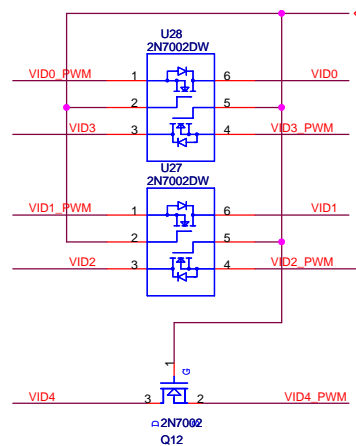


CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)
OCP=40A~45A

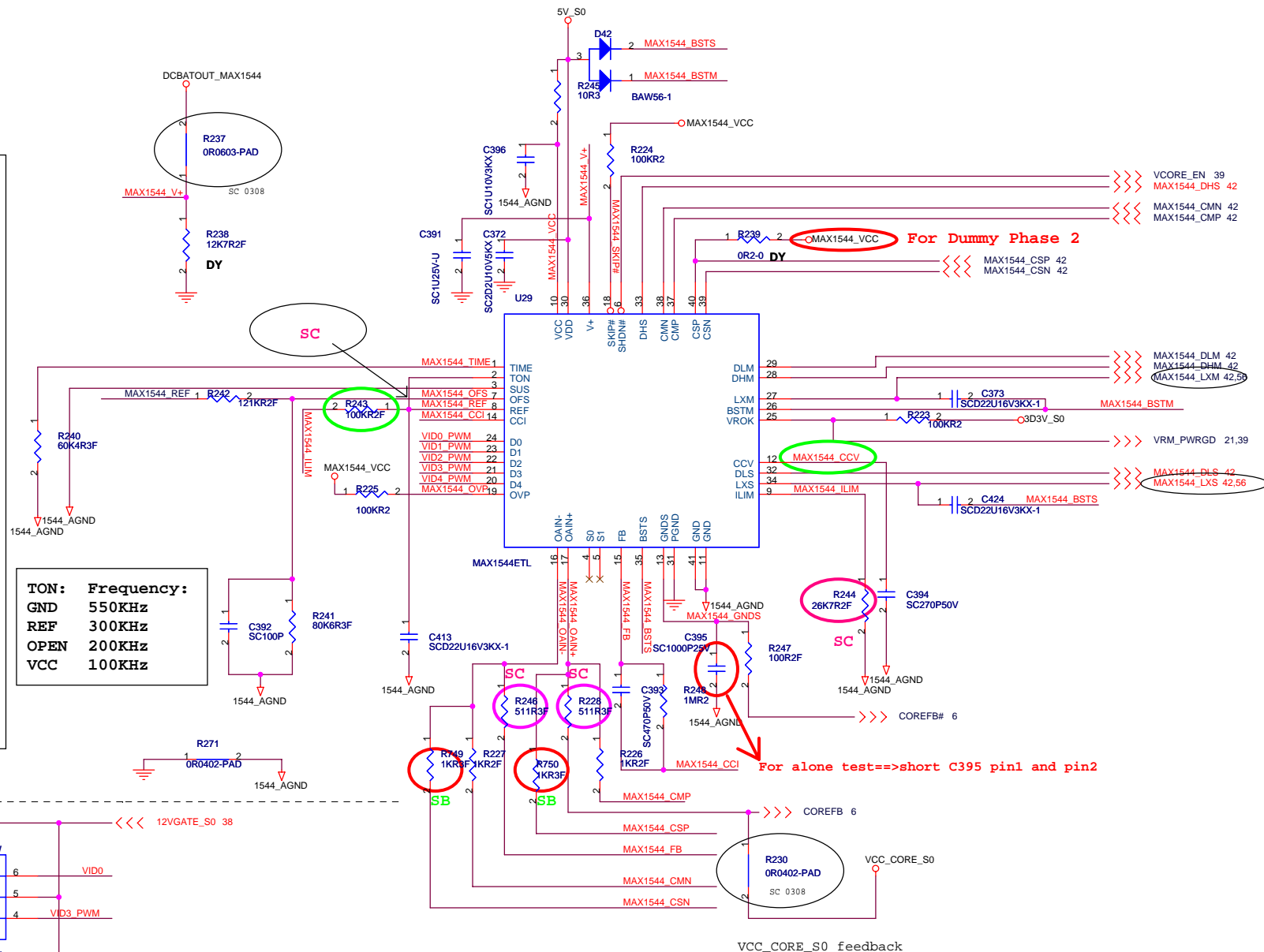
TABLE 1. VOLTAGE IDENTIFICATION CODES	
1	100
2	101
3	102
4	103
5	104
6	105
7	106
8	107
9	108
10	109
11	110
12	111
13	112
14	113
15	114
16	115
17	116
18	117
19	118
20	119
21	120
22	121
23	122
24	123
25	124
26	125
27	126
28	127
29	128
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72	171
73	172
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76	175
77	176
78	177
79	178
80	179
81	180
82	181
83	182
84	183
85	184
86	185
87	186
88	187
89	188
90	189
91	190
92	191
93	192
94	193
95	194
96	195
97	196
98	197
99	198
100	199

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz



From KBC



SC:

1. Change R246 and R228 to 511R3F(64.51105.651).
2. Change R224 to 26K7R2F(64.26725.6D1).
3. Cut off a trace between pin7 and pin8 of U29.

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih.

CPU Vcore 1

Size	Document Number
------	-----------------

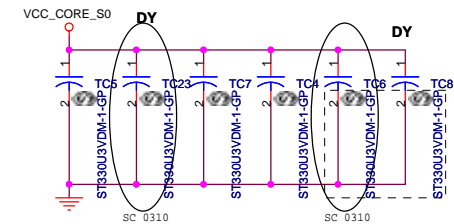
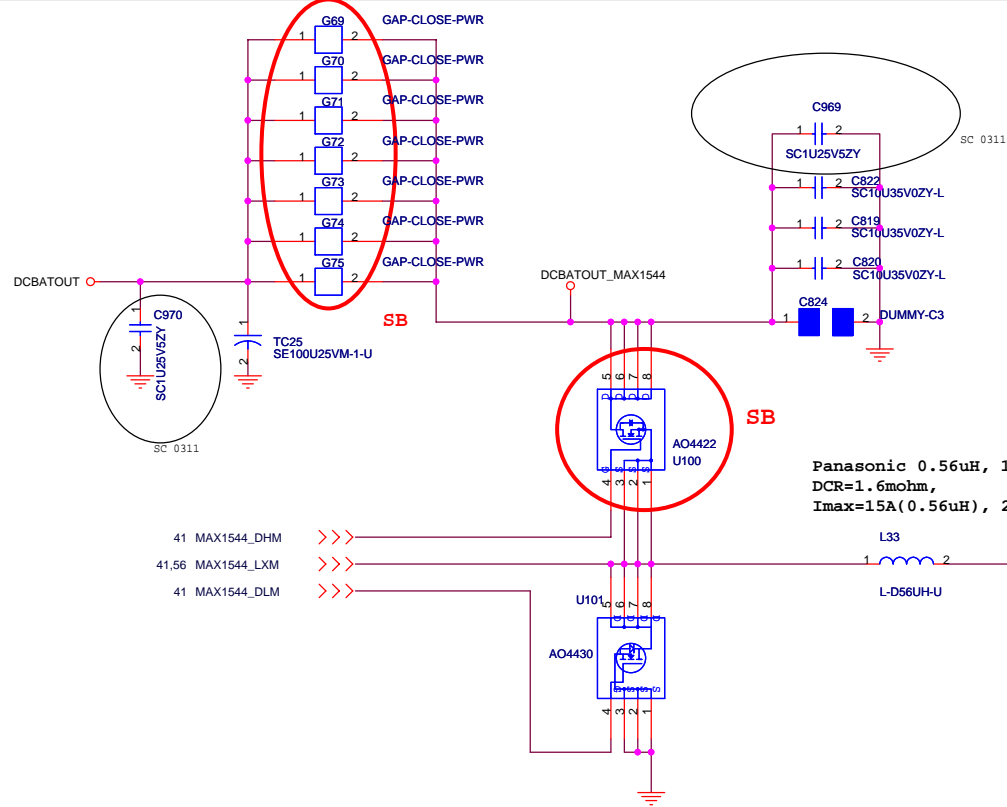
Bolsena

Rev

Date: Thursday, March 31, 2005

Sheet 41 of 58

(Power Team)



KEMET 330uF / 3V / 80.3371X.L02
ESR=9mohm / Irripple=3.7A
7.3/4.3/1.9, NT:9.0

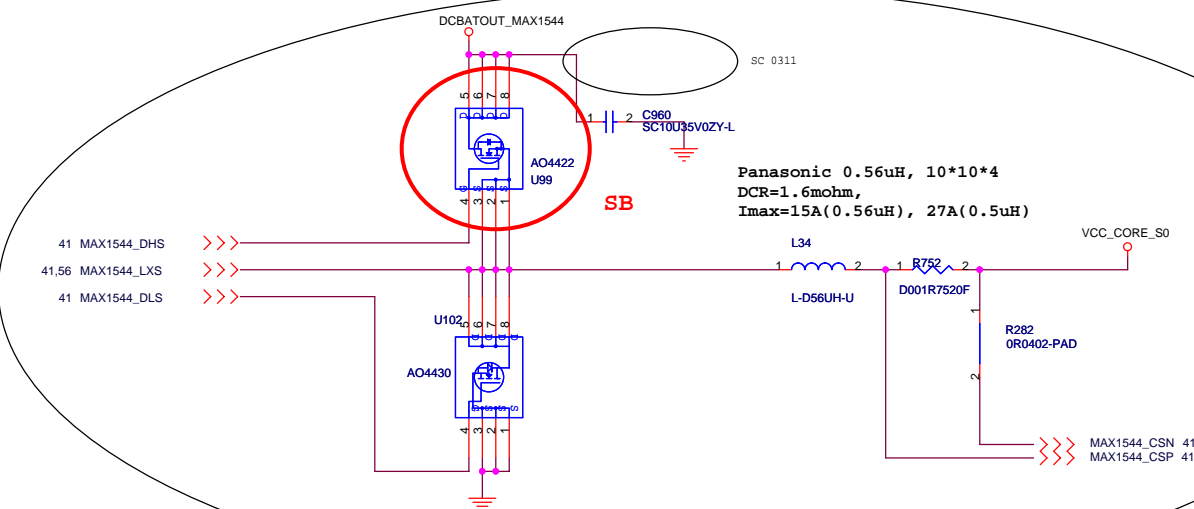
41 MAX1544_DHM
41,56 MAX1544_LXM
41 MAX1544_DLM

Panasonic 0.56uH, 10*10*4
DCR=1.6mohm,
Imax=15A(0.56uH), 27A(0.5uH)

R229
0R0402-PAD

Place 0R0402-PAD close to the resistor

MAX1544_CMN 41
MAX1544_CMP 41



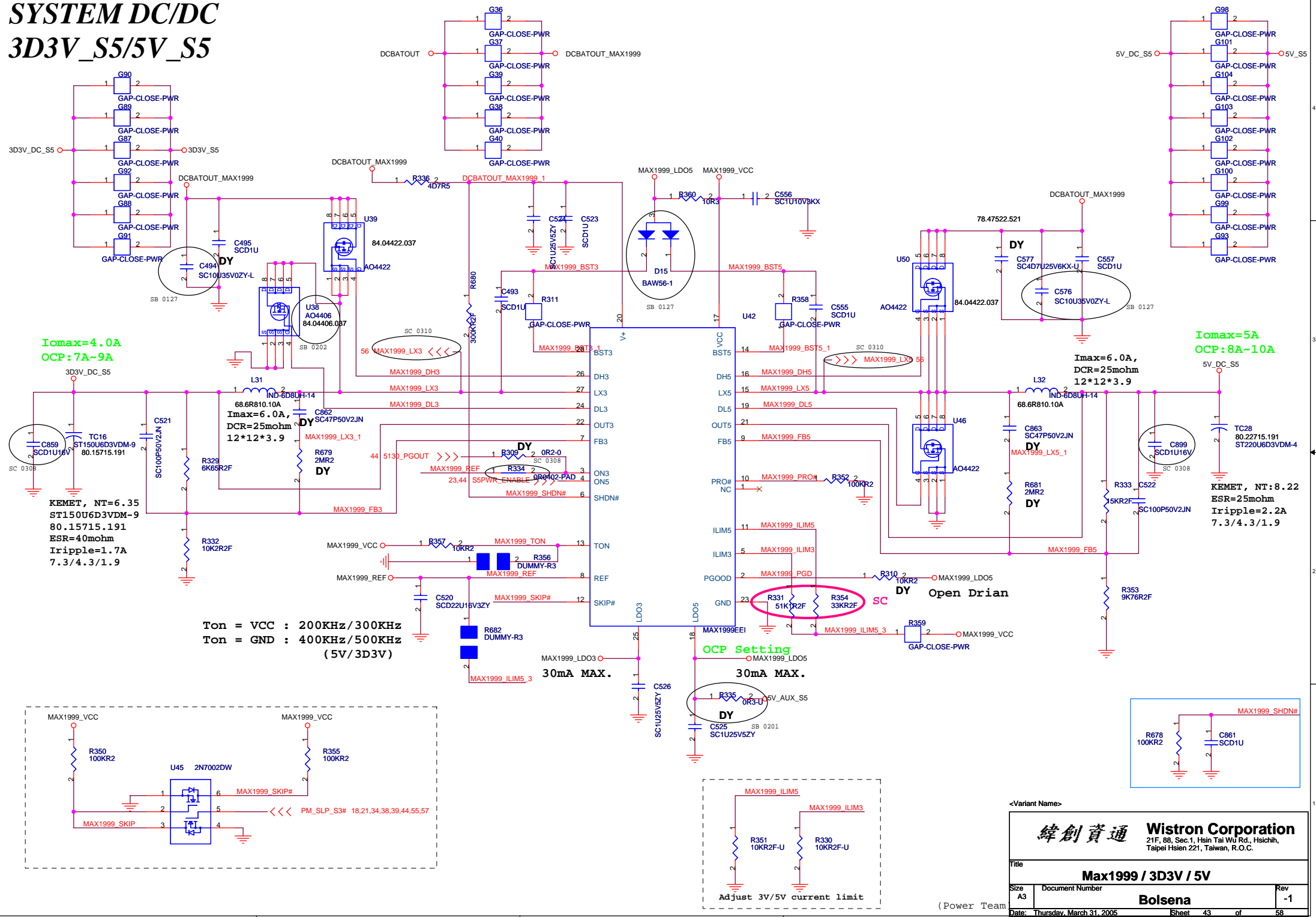
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU Vcore 2			
Size	Document Number		Rev
A3	Bolsena		-1
Date: Thursday, March 31, 2005		Sheet 42 of	58

(Power Team)

SYSTEM DC/DC
3D3V_S5/5V_S5



TI TPS5130 for 2.5V, 1.2V, 1.8V

$$V_o = (R1 \cdot 0.85) / R2 + 0.85$$

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)

For 1.2V
SETTING=1.2172V

PWM_SEL	Condition	Voltage
H	Auto PWM/SKIP	2.2V(Min)~
* L	PWM fixed (300KHz)	~0.3V(Max)

TPS5130

LDO SETTING

PWM_SEL	Condition	Voltage
H	Auto PWM/SKIP	2.2V(Min)~
* L	PWM fixed (300KHz)	~0.3V(Max)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

TPS5130 1D2V/1D8V2D5V/ (1/2)

Size A3 Document Number **Bolsena** Rev -1
Date: Thursday, March 31, 2005 Sheet 44 of 58

(Power Team)

WWW.AliSaler.Com

TI TPS5130 for 2D5V, 1D2V, 1D8V
(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)

D

44 5130_OUT1U
44,56 5130_LL1

44 5130_OUT1D

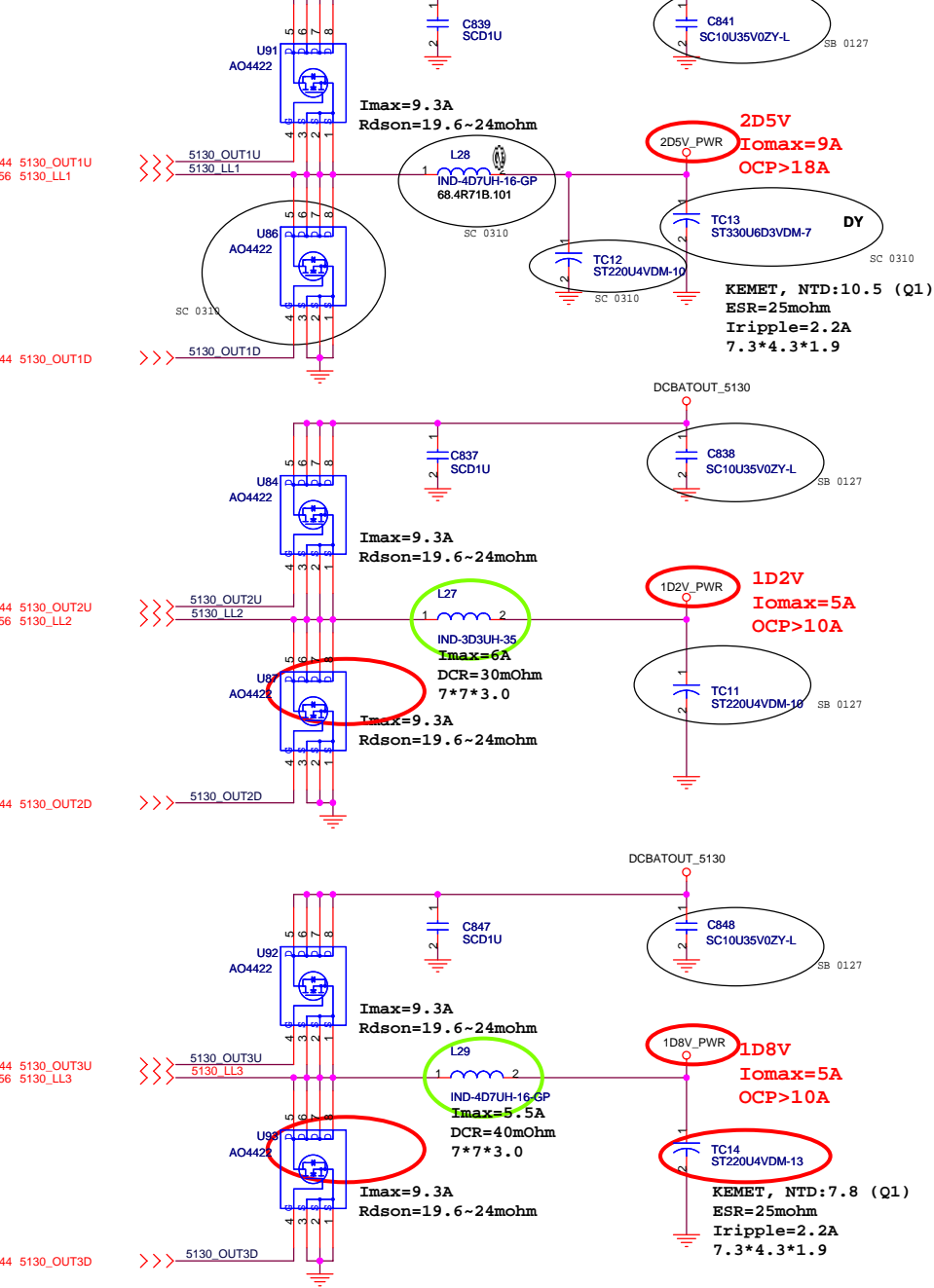
44 5130_OUT2U
44,56 5130_LL2

44 5130_OUT2D

44 5130_OUT3U
44,56 5130_LL3

44 5130_OUT3D

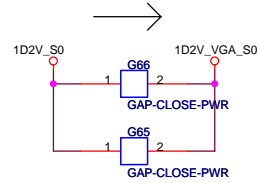
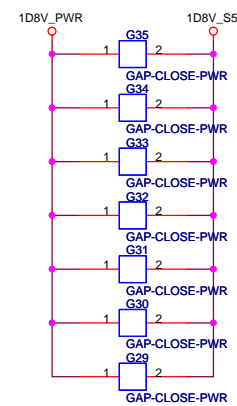
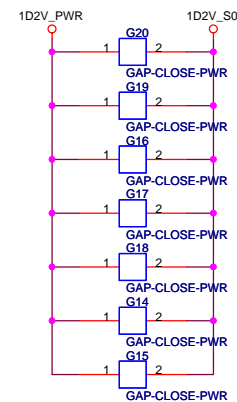
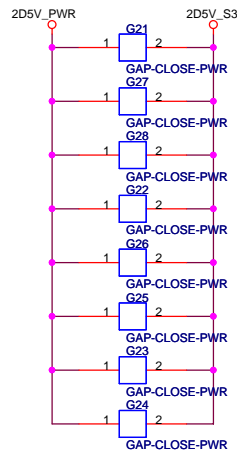
A



3

2

1

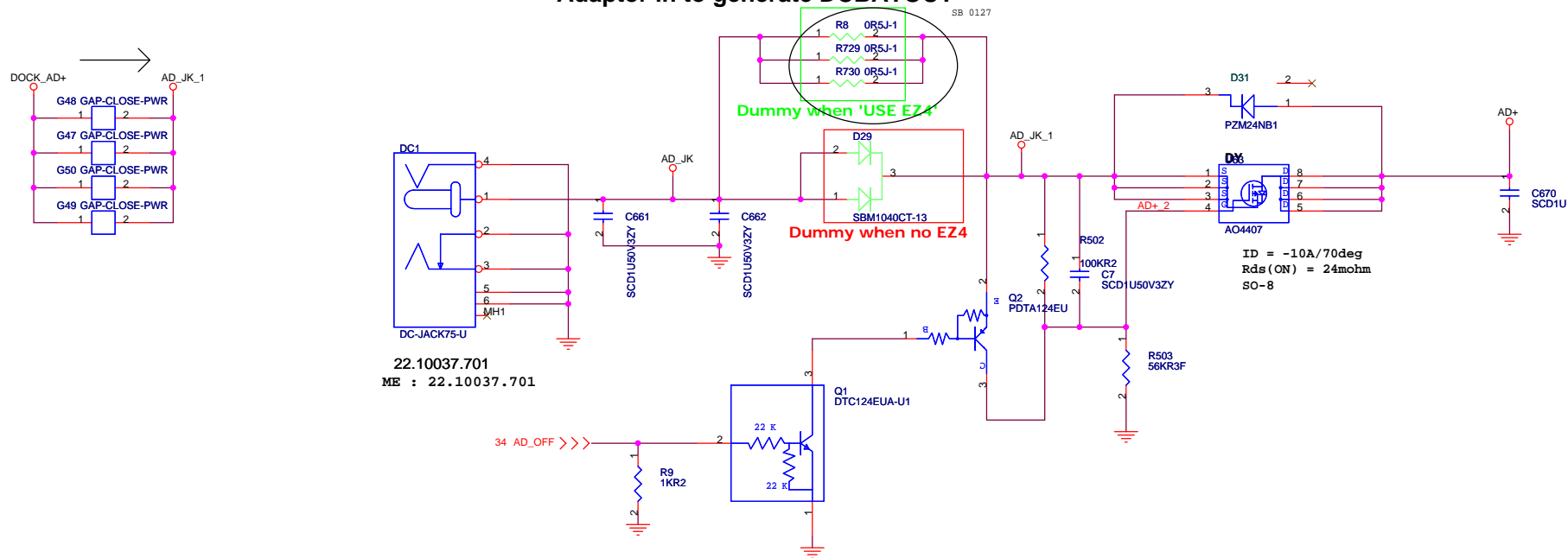


(Power Team)

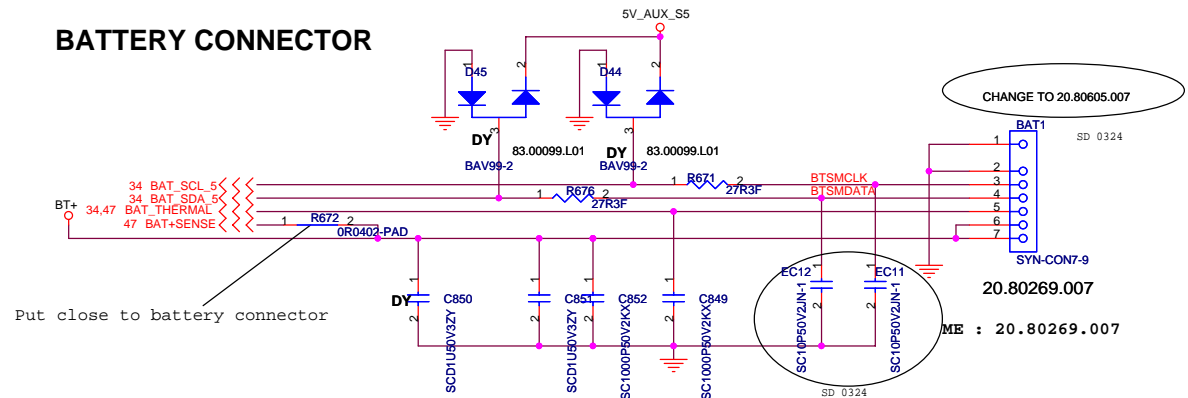
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title TPS5130 1D2V/1D8V2D5V/ (2/2)		
Size A3	Document Number Bolsena	Rev -1
Date: Thursday, March 31, 2005		Sheet 45 of 58

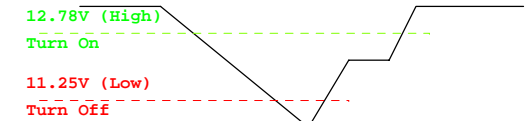
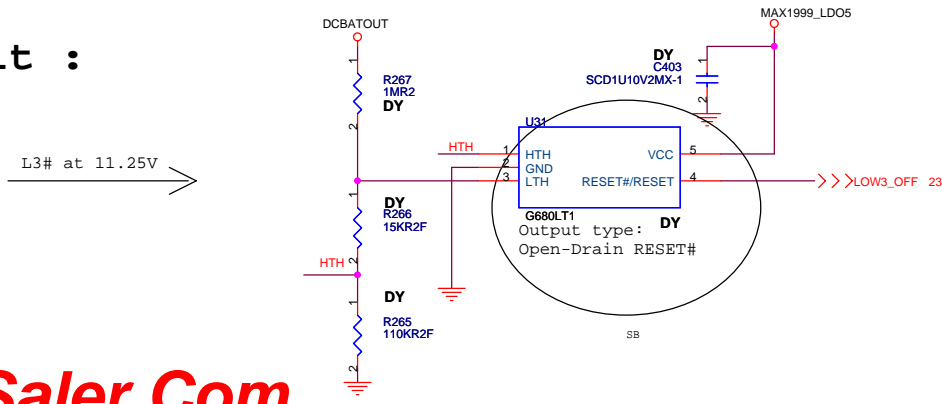
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



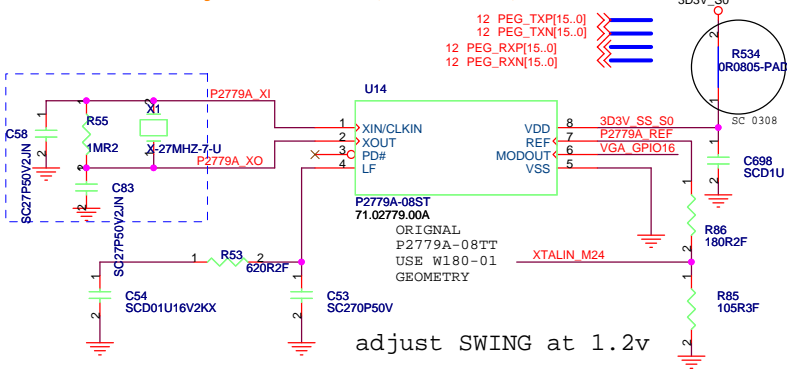
Low3 Circuit :



<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
AD/BATT CONN	
Size	Rev
A3 Document Number	-1
Bolsena	
Date: Thursday, March 31, 2005	Sheet 48 of 58

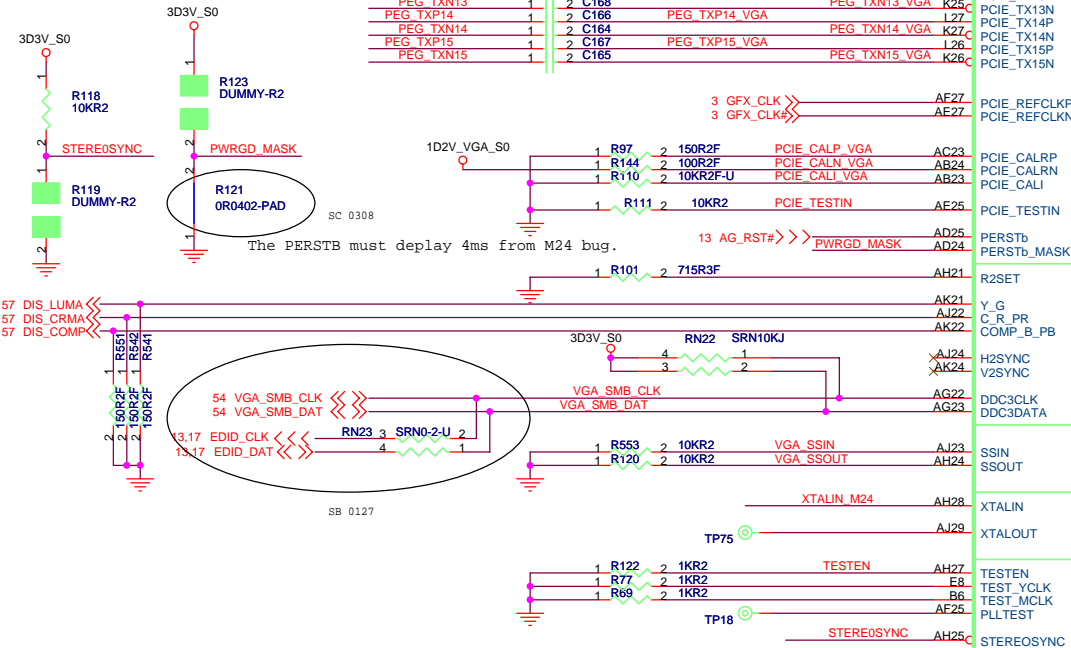
Dummy when use UMA (WHOLE PAGE)



adjust SWING at 1.2v

PEG_TXP0	1	2	C195	PEG_TXP0_VGA	PEG_TXN0_VGA	AE26
PEG_TXN0	1	2	C193	PEG_TXP1_VGA	PEG_TXN1_VGA	AE25
PEG_TXP1	1	2	C194	PEG_TXP2_VGA	PEG_TXN2_VGA	AE27
PEG_TXN1	1	2	C192	PEG_TXP3_VGA	PEG_TXN3_VGA	AE26
PEG_TXP2	1	2	C190	PEG_TXP4_VGA	PEG_TXN4_VGA	AE25
PEG_TXN2	1	2	C188	PEG_TXP5_VGA	PEG_TXN5_VGA	AE27
PEG_TXP3	1	2	C191	PEG_TXP6_VGA	PEG_TXN6_VGA	AE26
PEG_TXN3	1	2	C189	PEG_TXP7_VGA	PEG_TXN7_VGA	AE25
PEG_TXP4	1	2	C187	PEG_TXP8_VGA	PEG_TXN8_VGA	AE27
PEG_TXN4	1	2	C185	PEG_TXP9_VGA	PEG_TXN9_VGA	AE26
PEG_TXP5	1	2	C183	PEG_TXP10_VGA	PEG_TXN10_VGA	AE25
PEG_TXN5	1	2	C181	PEG_TXP11_VGA	PEG_TXN11_VGA	AE27
PEG_TXP6	1	2	C186	PEG_TXP12_VGA	PEG_TXN12_VGA	AE26
PEG_TXN6	1	2	C184	PEG_TXP13_VGA	PEG_TXN13_VGA	AE25
PEG_TXP7	1	2	C182	PEG_TXP14_VGA	PEG_TXN14_VGA	AE27
PEG_TXN7	1	2	C180	PEG_TXP15_VGA	PEG_TXN15_VGA	AE26
PEG_TXP8	1	2	C178			
PEG_TXN8	1	2	C176			
PEG_TXP9	1	2	C179			
PEG_TXN9	1	2	C177			
PEG_TXP10	1	2	C175			
PEG_TXN10	1	2	C173			
PEG_TXP11	1	2	C171			
PEG_TXN11	1	2	C169			
PEG_TXP12	1	2	C174			
PEG_TXN12	1	2	C172			
PEG_TXP13	1	2	C170			
PEG_TXN13	1	2	C168			
PEG_TXP14	1	2	C166			
PEG_TXN14	1	2	C164			
PEG_TXP15	1	2	C167			
PEG_TXN15	1	2	C165			

The PERSTB must delay 4ms from M24 bug.



SB 0127

M26-P-1 (M24)71.00M24.CO.U - (M26)71.0M26P.OOU

Part 1 of 6

DVO / EXT TMS / GPIO

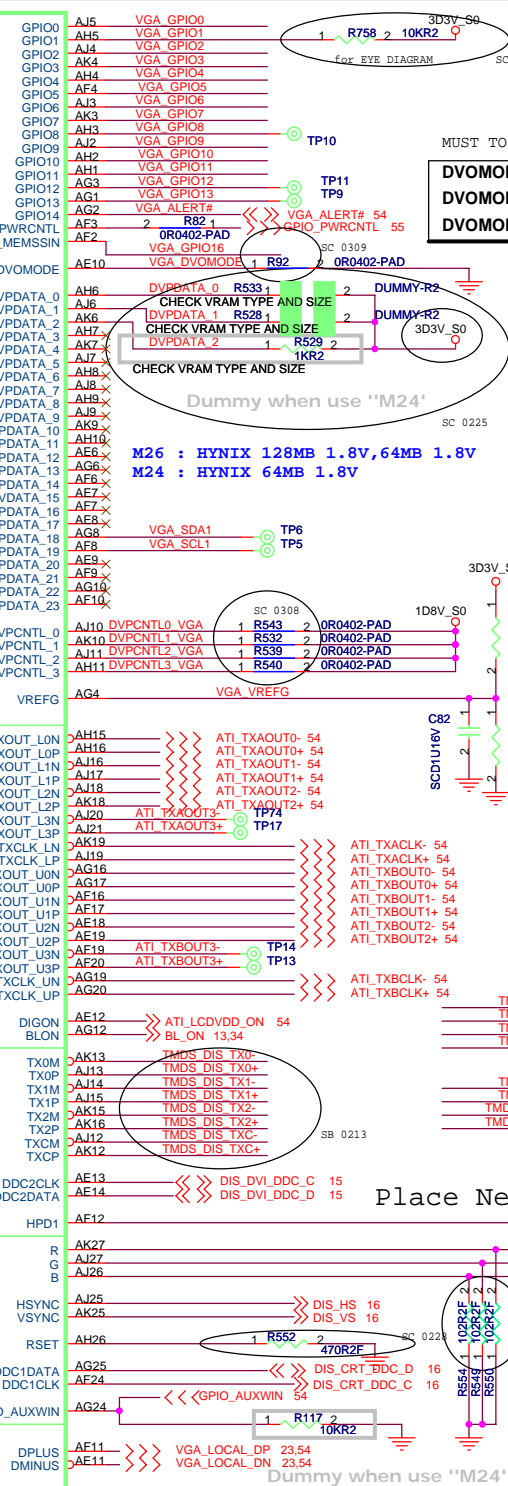
LVDS

TMDS

DAC1

CLK \$

THERM



Place Near To EZPORT4

Dummy when use "M24"

DVOMODE=VSS 3.3V MODE
DVOMODE=VDDC to 1.8V 1.8V MODE
DVOMODE=GND NO USE DVPPDATA

STRAPS	PIN	DEFAULT
CAL_BG_BACKUP	GPIO0	1
PLL_CAL_FORCE_EN	GPIO1	1
PCIE_MODE(1:0)	GPIO(3:2)	00 SE 0219
CAL_OFF	GPIO4	1
BYPASS_PLL	GPIO5	0 SE 0219
ICOMP	GPIO6	0
DEBUG_ACCESS	GPIO8	0
ROMIDCFG(3:0)	GPIO(9,13:11)	0000
MULTIFUNC(1:0)	LCDDATA(17:16)	0
VIP_DEVICE	LCDDATA(20)	0
DWNGRO	LCDDATA(21) (internal pull-down)	0

ATI Ref. Datasheets (page 3-32)
DOC.NO.: CHS-216M24-03
GPIO[0..13] are internal pull-down.

TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

DVDPDATA_2, 1, 0	0 0 0	64MB Hynix
	0 0 1	64MB Samsung
	0 1 0	64MB X brand
	0 1 1	64MB Y brand
	1 0 0	128MB Hynix
	1 0 1	128MB Samsung
	1 1 0	128MB X brand
	1 1 1	128MB Y brand

TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

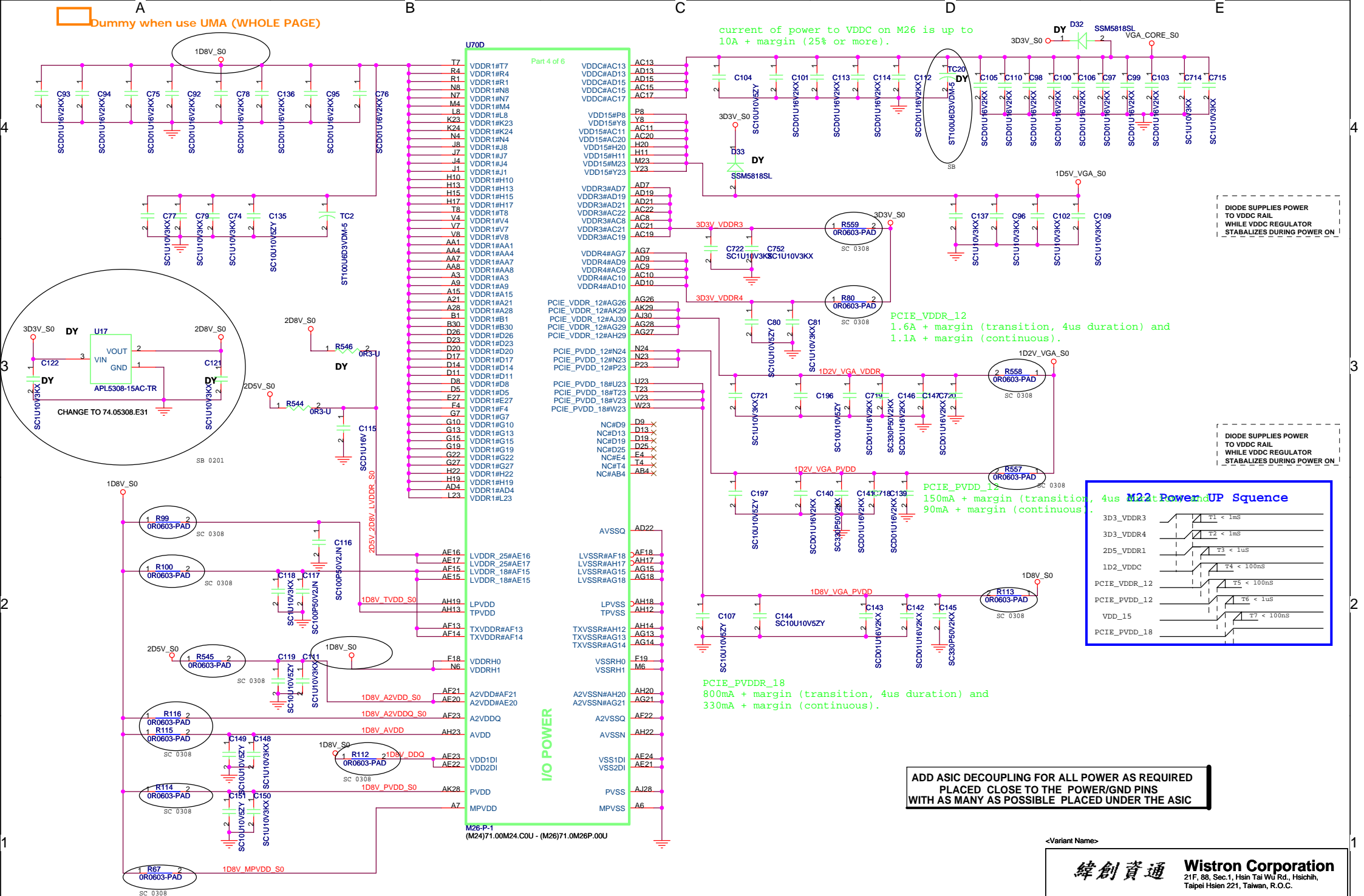
TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

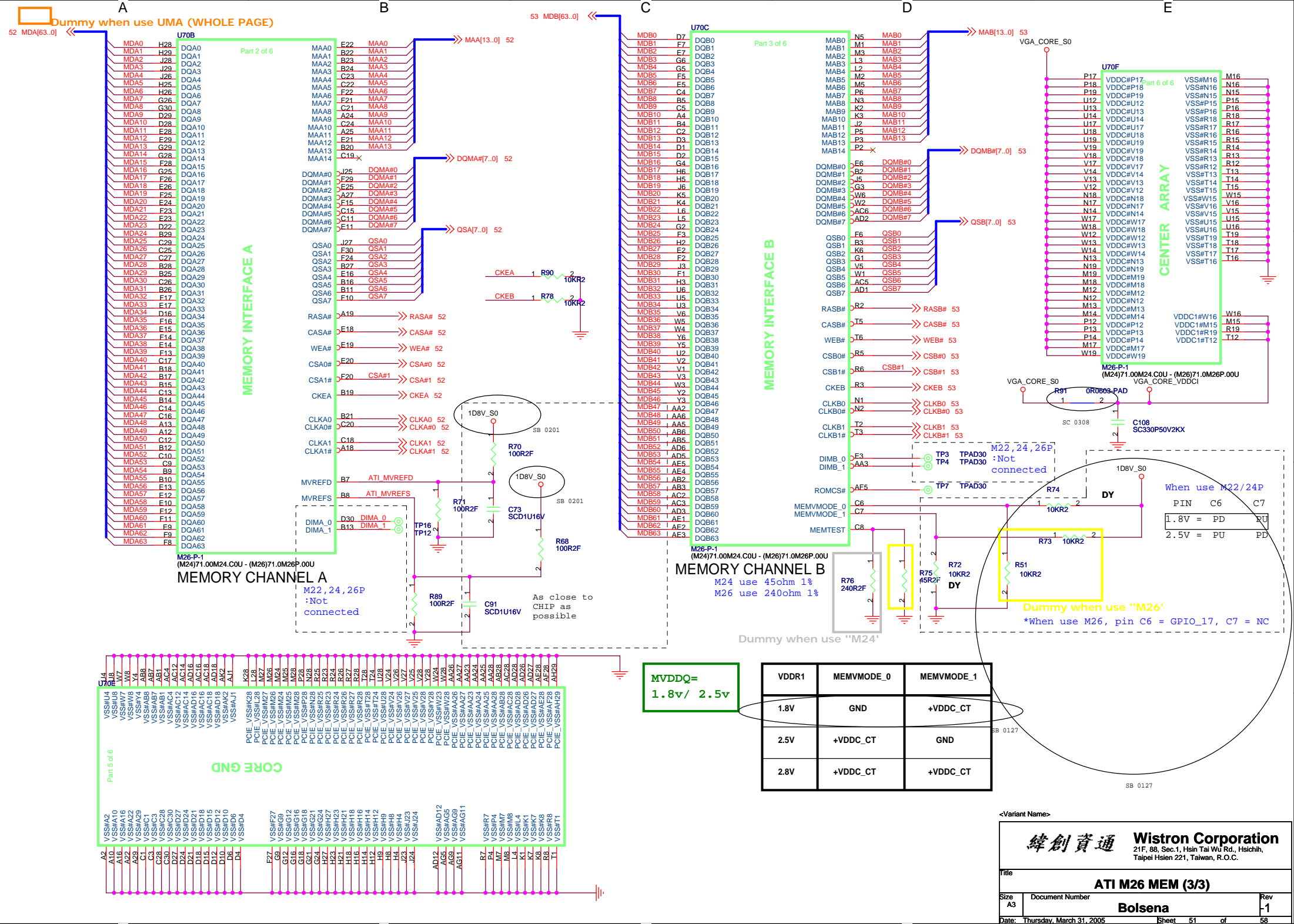
TMDS DIS TX0- 1 R95 2 330R2 TMDS DIS TX0+
TMDS DIS TX1- 1 R96 2 330R2 TMDS DIS TX1+
TMDS DIS TX2- 1 R97 2 330R2 TMDS DIS TX2+
TMDS DIS TX3- 1 R98 2 330R2 TMDS DIS TX3+

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi,
Taipei Hsien 221, Taiwan, R.O.C.

ATI M26 PCIE LVDS (1/3)
Bolsena
Date: Thursday, March 31, 2005 Sheet 49 of 58

Dummy when use UMA (WHOLE PAGE)





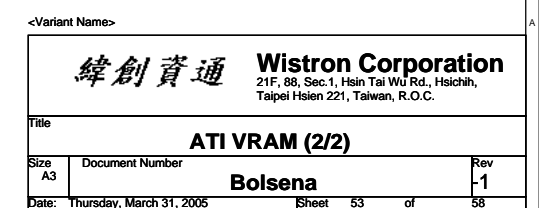
All dampings in this page must near the VRAM.

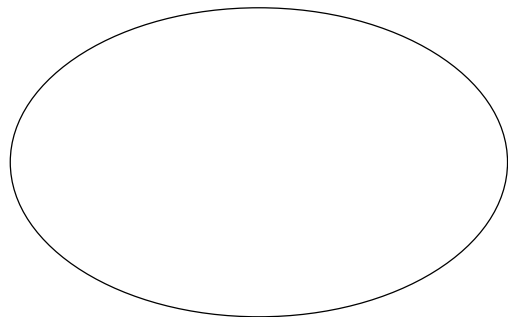


58

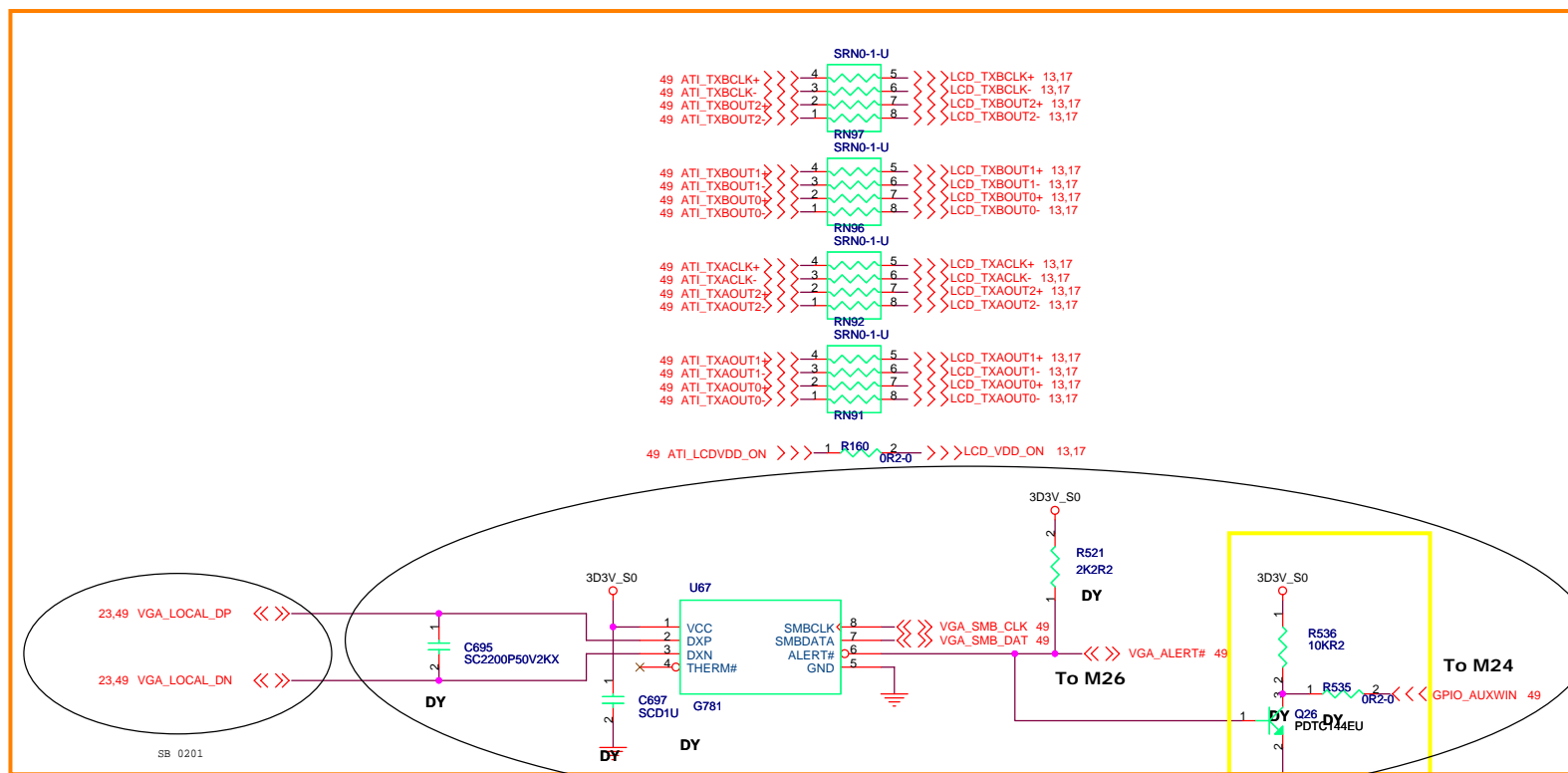
WWW.AliSaler.Com

☐ Dummy when use UMA (WHOLE PAGE)





SB 0201



SB 0201

Dummy when use UMA

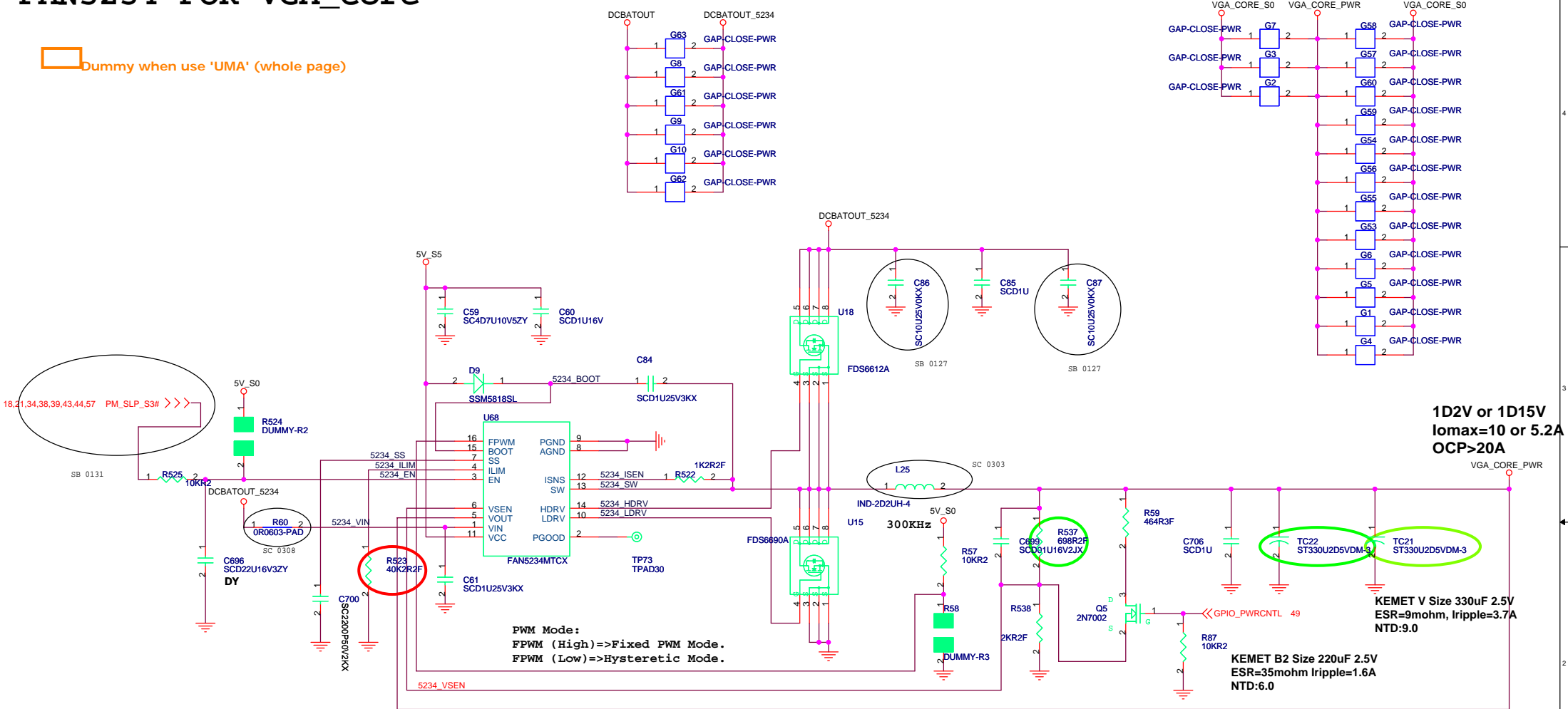
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

VGA SELECTOR		
Title	VGA SELECTOR	
Size	Document Number	Rev
A3	Bolsena	1
Date	Thursday, March 31, 2005	Sheet 54 of 58

FAN5234 FOR VGA_Core

Dummy when use 'UMA' (whole page)

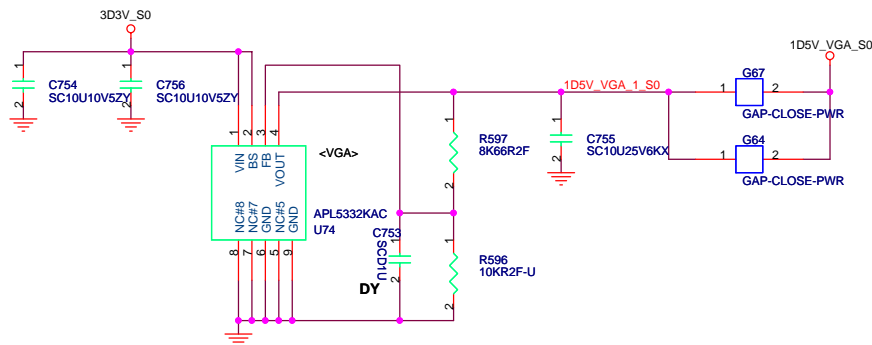


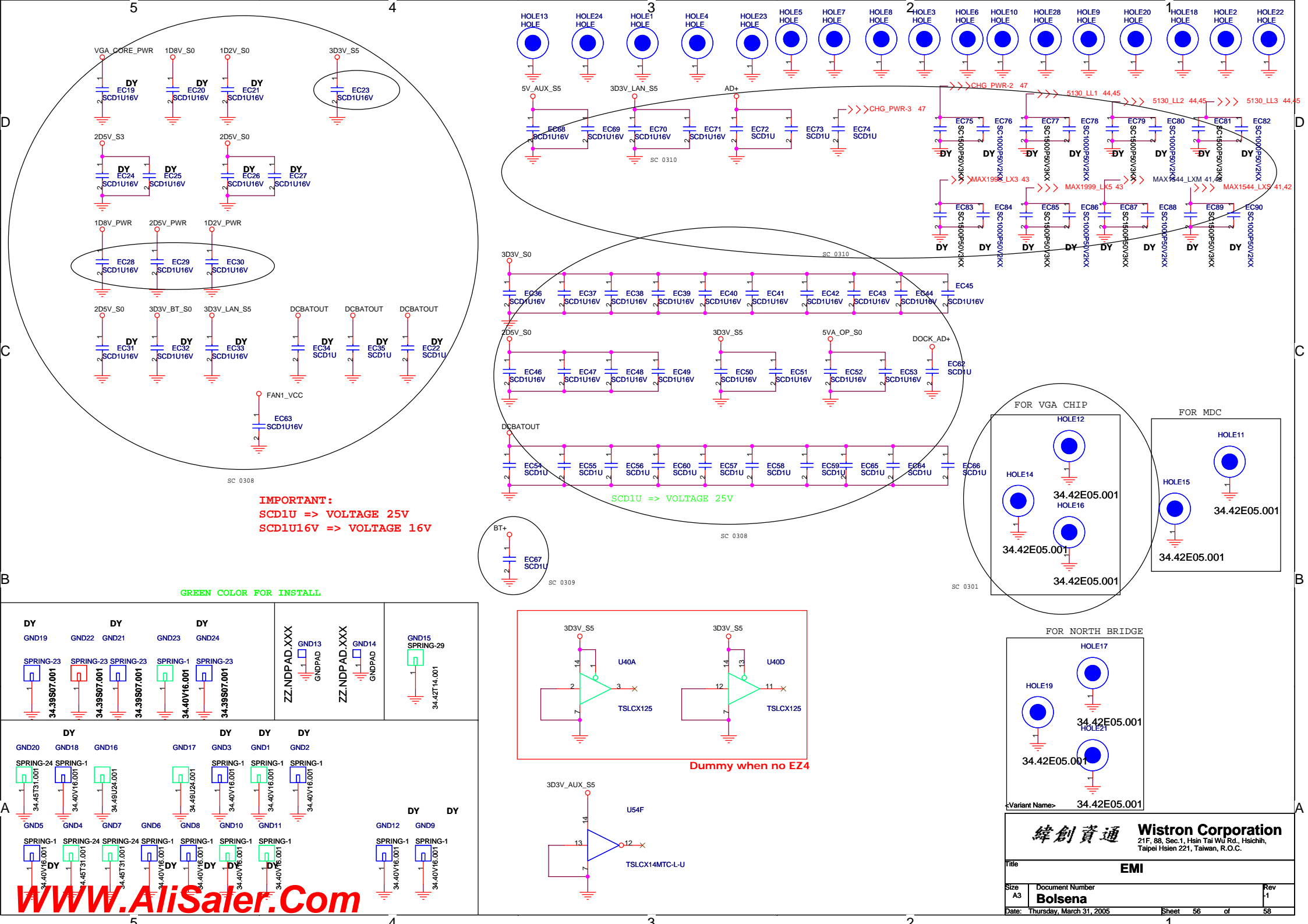
$$R_{ilim} = (11.2 / I_{lim}) * ((100 + R_{sense}) / R_{dson})$$

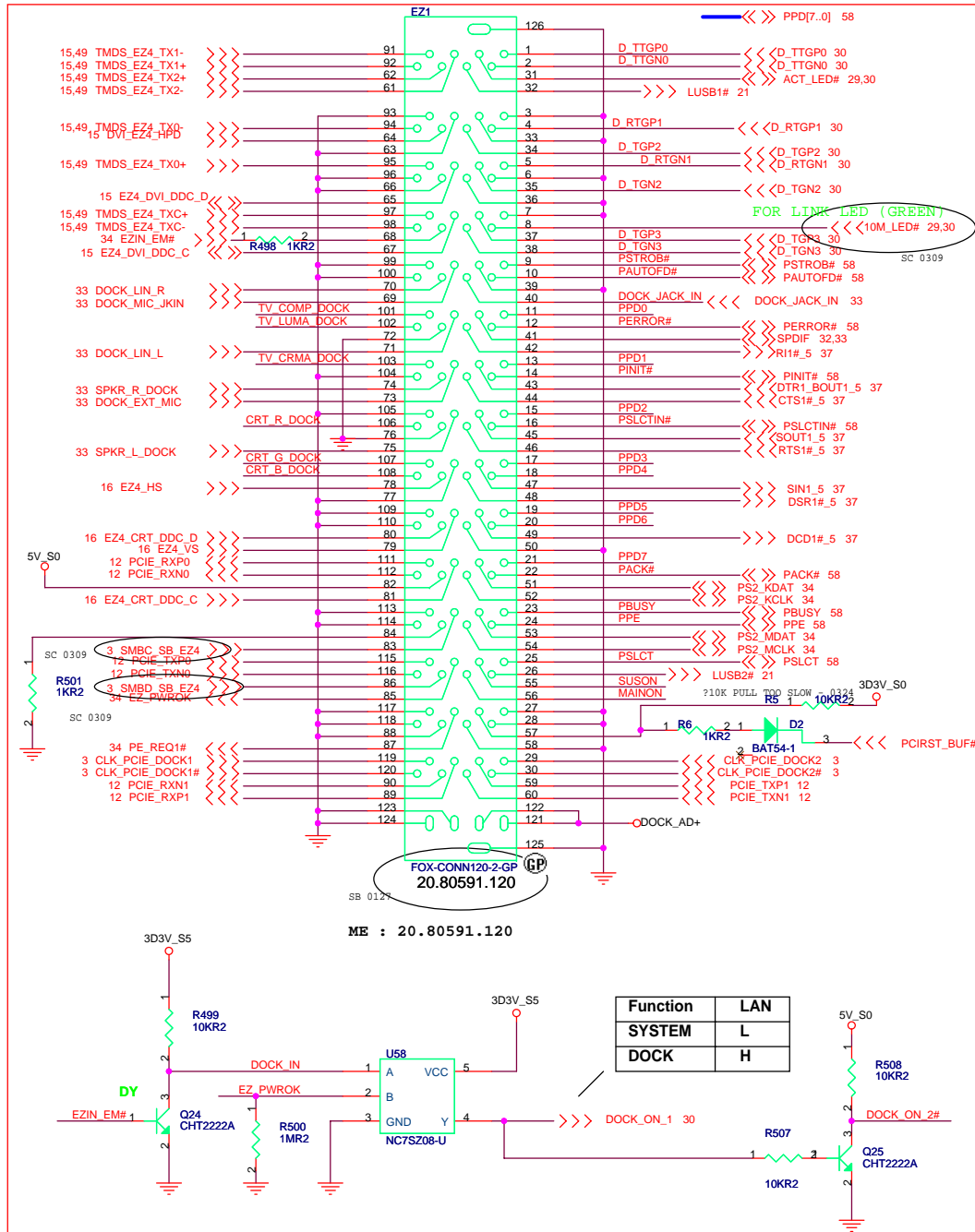
High (3.3V) => Vo=1.0V
Low (0V) => Vo=1.2V

Vout Setting:
0.9V/Rlow=(Vout-0.9V)/Rhigh

M24/M26 POWER PLAY (GPIO_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)



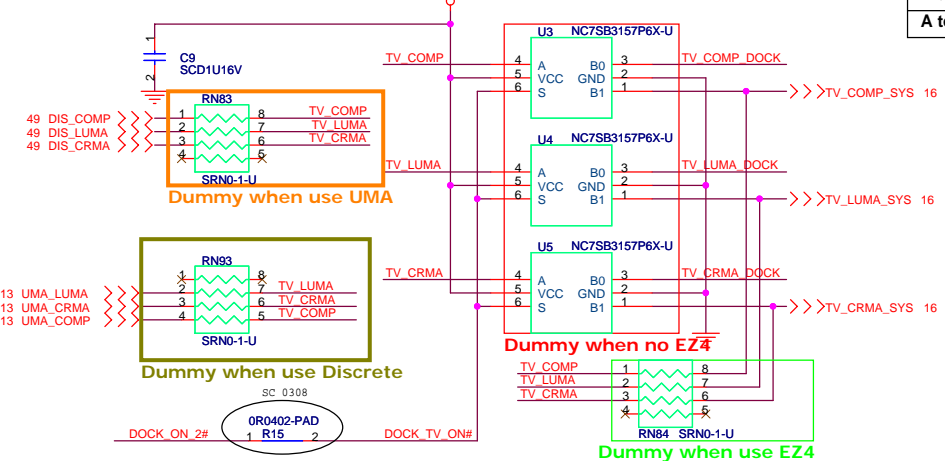




Dummy when no EZ4

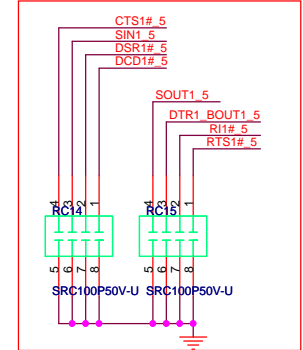
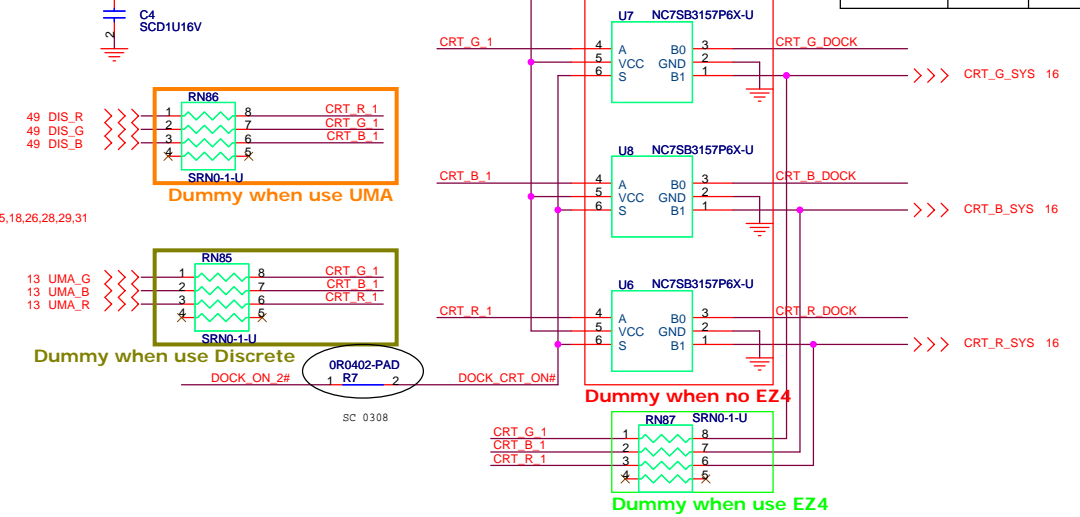
TV SWITCH

Function	S
A to B0	L
A to B1	H



CRT SWITCH

Function	CRT	TV
SYSTEM	H	H
DOCK	L	L



Dummy when no EZ4

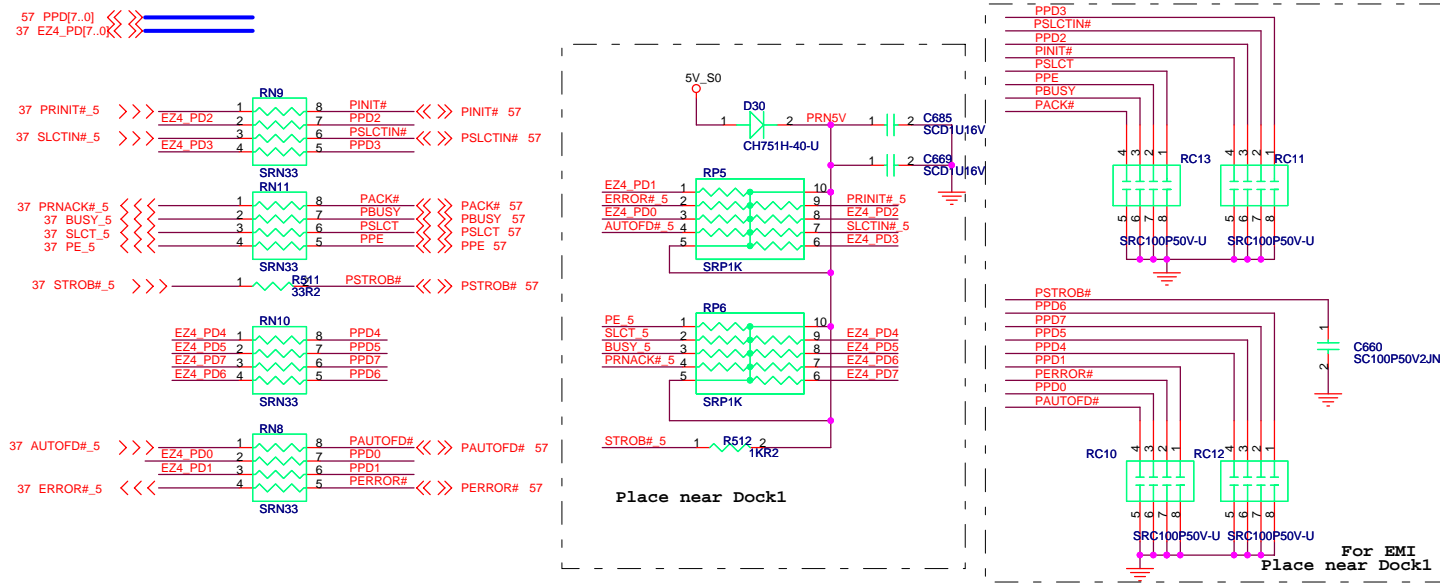
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EASY PORT4 (1/2)**

Size A3 Document Number: **Bolsena** Rev: **-1**

Date: Thursday, March 31, 2005 Sheet 57 of 58

PRINT PORT



Dummy when no EZ4

